Service
Service
Service

Service Manual

CLASS 1
LASER PRODUCT

DVD VIDEO

COMPACT disc DIGITAL VIDEO

COMPACT disc DIGITAL AUDIO

Contents **Page**

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PHILIPS

1. Technical Specifications

1.1 Interfaces and Pin Assignments

The interfaces or connectors are placed on both PCB layers of top and bottom as shown in figure "Interfaces placement on PCB layer".

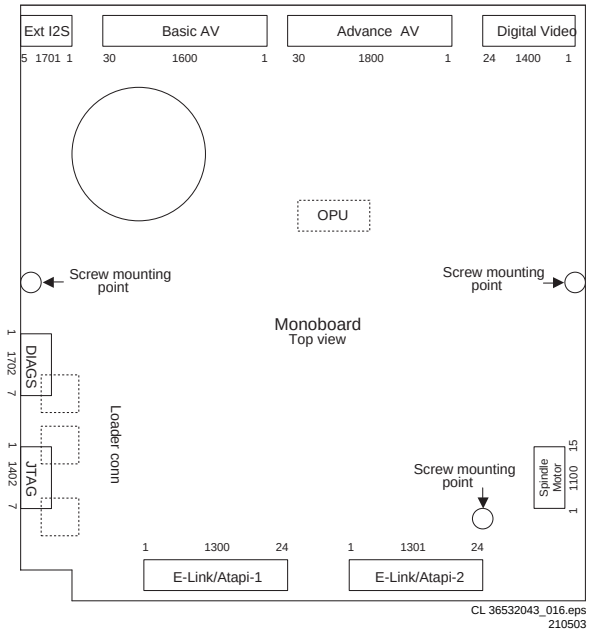


Figure 1-1 Interfaces placement on PCB layer

1.2 Connections

1.2.1 Interface ADVANCE AV at Location 1800:

1. I2CSCL_M / I2CSCL_S
2. I2CSDA_M / I2CSDA_S
3. SCART1 / I2C INT/ GND
4. SCART0 / SLOT_IN_DET
5. B_REF (Video ground)
6. B_U
7. G_REF (Video ground)
8. G_Y
9. R_REF (Video ground)
10. R_V
11. Y_REF (Video ground)
12. Y
13. C_REF (Video ground)
14. C
15. CVBS-REF (Video ground)
16. CVBS
17. +3V3
18. +3V3
19. +5V
20. +12V_Stby
21. +12V
22. MUTE / SPDIF
23. GND
24. PCMSCLK
25. PCMDATA0 / Lt
26. GND_LRT (Audio ground)
27. PCMCLK / Rt
28. PCMLRCLK
29. GND
30. SPDIF / MUTE

1.2.2 Interface Basic AV at Location 1600

1. GND
2. DVD_SC
3. GND_SC
4. DVD_L
5. GND_L
6. DVD_R/ PCMDATA3(CELf)
7. GND_R
8. DVD_LFE
9. GND_LFE
10. DVD_LS / PCMDATA2(LsRs)
11. GND_LS
12. DVD_C
13. GND_C
14. DVD_RS/ PCMDATA1(LR)
15. GND_RS
16. SENSE_3V3
17. GND
18. MIC_IN (KOK)
19. GND
20. VIDEO_SEL
21. GND
22. I2CSCL_M
23. I2CSDA_M
24. GND
25. PCMDATA0(LtRt)
26. GND
27. DIG_IN_1
28. I2C INT
29. DAC_RST
30. GND

1.2.3 Service connector at Location 1702:

1	TXD_SER	TXD service UART
2	SERVICE	Service or normal mode select
3	RXD_SER	RXD service UART
4	RTS_SER	Not used
5	GNDB	Ground
6	CTS_SER	Not used
7	+5V	5V supply

1.3 Signal Specifications

This section defines the specifications of the signals at the module interface.

1.3.1 Voltage level

TTLTransistor-transistor logic (5V logic)

Caution: Exceeding the absolute maximum rating will cause damage to the module.

Absolute maximum rating:
IN =-0.5V to 5.5V
VOUT = -0.5V to 5.5V

Table 1-1

Parameter	Min	Max
VIH (V)	2.0	-
VIL (V)	-	0.8
VOH (V)	2.4	-
VOL (V)	-	0.4

LVTTLLow voltage transistor-transistor logic (3.3V logic)

Caution: Exceeding the absolute maximum rating will cause damage to the module.

Absolute maximum rating:
VIN = -0.5V to 3.8V
VOUT =-0.5V to 3.8V

Maximum current drive: 4mA

Table 1-2

Parameter	Min	Max
VIH (V)	2.0	-
VIL (V)	-	0.8
VOH (V)	2.4	-
VOL (V)	-	0.4

I2C
- Inter-IC
- All I2C signals at the module's connectors are 5V levels.

I2S
- Inter-IC sound
- All I2S signals at the module's connectors are at LVTTL levels.

RS232_COMP
- RS232 compatible specifications
- VIN approximately 3V threshold, 6kohm input resistance
- VOUT = 0 to 5V, 1kohm output resistance

H/L
- 5V logic states
- H = +5V ± 0.5V
- L = 0V ± 0.5V

h/l
- 3.3V logic states
- h = +3.3V ± 0.3V
- l = 0V ± 0.3V

1.3.2 SPDIF out

Function : Digital audio output
Signal : SPDIFOUT
Type : Output according to IEC60958 or IEC61937, 1Vp-p, unbalanced.

1.3.3 Audio PCM (I2S format)

Function : Digital audio
Signal : DA_XCK, DA_BCK, DA_LRCK, DA_DATA0, DA_DATA1, DA_DATA2, DA_DATA3
Type : I2S output (33ohm output resistors, in series)

1.3.4 Analog Audio

Function : Analog audio, 2-ch
Signal : LT, RT
Type : Analog output with on-bd. 10k load

1.3.5 Audio mute

Function : Audio mute control for final analog stage
Signal : MUTE
Type : LVTTL output

Table 1-3

Function	MUTE
Mute off	LOW
Mute on	HIGH

1.3.6 Analog video

Function : Analog video
Signal : CVBS_VID, C_VID, Y_VID, R_VID (V), G_VID (Y), B_VID (U)
Type : Output (75ohm output resistors, in series)

1.3.7 Slow blanking SCART

Function : Slow blanking SCART (0/6/12)
Signal : SCART0, SCART1
Type : LVTTL output

Table 1-4

Function	SCART0	SCART1
TV display	HIGH	HIGH
TV display	LOW	HIGH
16:9 aspect ratio	HIGH	LOW
4:3 aspect ratio	LOW	LOW

Note: SCART0 & SCART1 are legacy features. They were used to generate 0/6/12 signal on an ext. A/V bd. However, most TV/Audio sets have their own Scart control ic & hence these 2 pins have alternate functions via optional jumpers. SCART1 shares with I2C_INT & GND; SCART0 pin shares with SLOT_IN_DETECT.

1.3.8 Slave I2C

Function : Slave I2C bus (Hardware)
Signal : S_I2C_CL; S_I2C_DA
Type : I2C

Note: I2C lines are pulled to +5V.

1.3.9 Master I2C

Function : Master I2C bus (Software)
Signal : M_I2C_CL; M_I2C_DA
Type : I2C

Note: I2C lines are pulled to +5V.

1.3.10 27MHz clock

Function : Output a 27MHz clock signal
Signal : VCLK
Type : LVTTL output (100ohm output resistor, in series)

Note: This VCLK pin has dual functionality. It provides 27 Mhz when Digital video output is used & as
This VCLK pin has dual functionality. It provides 27 Mhz when Digital video output is used & as an input for PCM_CLK when ext. I2S is used. Option jumpers are provided.

Exercise caution when connecting to this line; excessive loading can cause noise and increase jitter levels & degrade the quality of SPDIF and I2S signals.

1.3.11 Service bus

Function : Service and diagnostic bus
Signal : TXD_SER, RXD_SER
Type : RS232_COMP (TXD_SER output, RXD_SER input)

1.3.12 Service activation

Function : To activate service/ diagnostic mode
Signal : SERVICE
Type : LVTTL input

Table 1-5

Function	SERVICE
Service mode	LOW (or pulled to ground)
Normal mode	HIGH (or unconnected)

Note: This line is pulled to HIGH via 10kohm resistor. A module reset is required to activate service mode.

1.4 Audio Format (I2S)

Function : Digital audio
Signal : DA_XCK, DA_BCK, DA_LRCK, DA_DATA0, DA_DATA1, DA_A
Additional 2 channels : downmixed stereo/ LtRt - optional
Sampling rate : MPEG-1, MPEG-2, Dolby Digital, DTS and DVD-Audio up to 192 kHz
Decoding : MPEG-1 and -2, Layers I, II, and III (MP3); MPEG-2 5.1;
: Dolby Digital Class A; MLP; DTS; Dolby Pro Logic; HDCD
Copy protection : CPPM for prerecorded media (DVD-audio)
: CPRM for recordable media (DVD-audio)
: Watermark detect and decode for DVD-audio

1.4.1 Analog video performance

The video output standard follows the source material. The OSD can be switched between PAL and NTSC.
The module has 6 analog video outputs in 4 format: CVBS, Y/C, and RGB (YUV). However, depending on the module configuration, not all output can be available at the same time.

Table 1-6

Signal name	Video format
CVBS_VID	CVBS
Y_VID, C_VID	Y/C
R_VID (V) / G_VID (Y) / B_VID (U)	RGB (YUV)

1.4.2 Option Jumpers:

J1, J2 & J3 hard select the required video output on Connector 1800. Alternatively, pre-determined Software setting, via slash option, is also possible. DAC's that are not in used should be turned off.
Note: RGB and YUV component video signals shared the same lines. Therefore, the module is not able to output both RGB and YUV at the same time.
Superimposed DC level : 1.2V
Output impedance : 75ohm

Signal-to-noise ratio : better than 65dB
Video bandwidth : 8MHz (± 3dB) / 16MHz (± 3dB) for progressive scan

Copy protection : CSS
: Macrovision Version 7.1.L.1 for NTSC/PAL interlaced video outputs
: Macrovision AGC 1.03 for 480P progressive scan video output

2. Safety Instructions, Warnings, and Notes

2.1 Safety Instructions

2.1.1 General Safety

Safety regulations require that during a repair:
- Connect the unit to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol ⚠, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that after a repair, you must return the unit in its original condition. Pay, in particular, attention to the following points:
- Route the wires/cables correctly, and fix them with the mounted cable clamps.
- Check the insulation of the mains lead for external damage.
- Check the electrical DC resistance between the mains plug and the secondary side:
  1. Unplug the mains cord, and connect a wire between the two pins of the mains plug.
  2. Set the mains switch to the 'on' position (keep the mains cord unplugged!).
  3. Measure the resistance value between the mains plug and the front panel, controls, and chassis bottom.
  4. Repair or correct unit when the resistance measurement is less than 1 MΩ.
  5. Verify this, before you return the unit to the customer/ user (ref. UL-standard no. 1492).
  6. Switch the unit 'off', and remove the wire between the two pins of the mains plug.

2.1.2 Laser Safety

This unit employs a laser. Only qualified service personnel may remove the cover, or attempt to service this device (due to possible eye injury).

Laser Device Unit

Type	:	Semiconductor laser GaAlAs
Wavelength	:	650 nm (DVD)
	:	780 nm (VCD/CD)
Output Power	:	20 mW (DVD+RW writing)
	:	0.8 mW (DVD reading)
	:	0.3 mW (VCD/CD reading)
Beam divergence	:	60 degree

Figure 2-1

Note: Use of controls or adjustments or performance of procedure other than those specified herein, may result in hazardous radiation exposure. Avoid direct exposure to beam.

2.2 Warnings

2.2.1 General

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD, ⚠). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are at the same potential as the mass of the set by a wristband with resistance. Keep components and tools at this same potential. Available ESD protection equipment:
  – Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
  – Wristband tester 4822 344 13999.
- Be careful during measurements in the live voltage section. The primary side of the power supply (pos. 1005), including the heatsink, carries live mains voltage when you connect the player to the mains (even when the player is 'off'!). It is possible to touch copper tracks and/or components in this unshielded primary area, when you service the player. Service personnel must take precautions to prevent touching this area or components in this area. A 'lightning stroke' and a stripe-marked printing on the printed wiring board, indicate the primary side of the power supply.
- Never replace modules, or components, while the unit is 'on'.

2.2.2 Laser

- The use of optical instruments with this product, will increase eye hazard.
- Only qualified service personnel may remove the cover or attempt to service this device, due to possible eye injury.
- Repair handling should take place as much as possible with a disc loaded inside the player.
- Text below is placed inside the unit, on the laser cover shield:

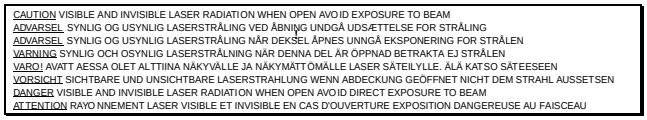


Figure 2-2

2.2.3 Notes

Dolby

Manufactered under licence from Dolby Laboratories. "Dolby", "Pro Logic" and the double-D symbol are trademarks of Dolby Laboratories. Confidential Unpublished Works. ©1992-1997 Dolby Laboratories, Inc. All rights reserved.

Figure 2-3

Trusurround

TRUSURROUND, **SRS** and symbol (fig 2-4) are trademarks of SRS Labs, Inc. TRUSURROUND technology is manufactured under licence frm SRS labs, Inc.

Figure 2-4

3. Directions for Use

There is no DFU available

4. Mechanical Instructions

4.1 Dismantling Instruction

Dismantling Instruction

1. Unplug 3 conn [C] from Monoboard [D].
2. Unlock conn 1100 on Monoboard [D] and gentlely unplug Flex [B].
3. Remove 3 screws [F].
4. Separate Monoboard [D] gentlely from loader [E] and beware of the Flex [A].
5. Unlock conn 1001 on the Monoboard [D] and gentlely unplug Flex [A].

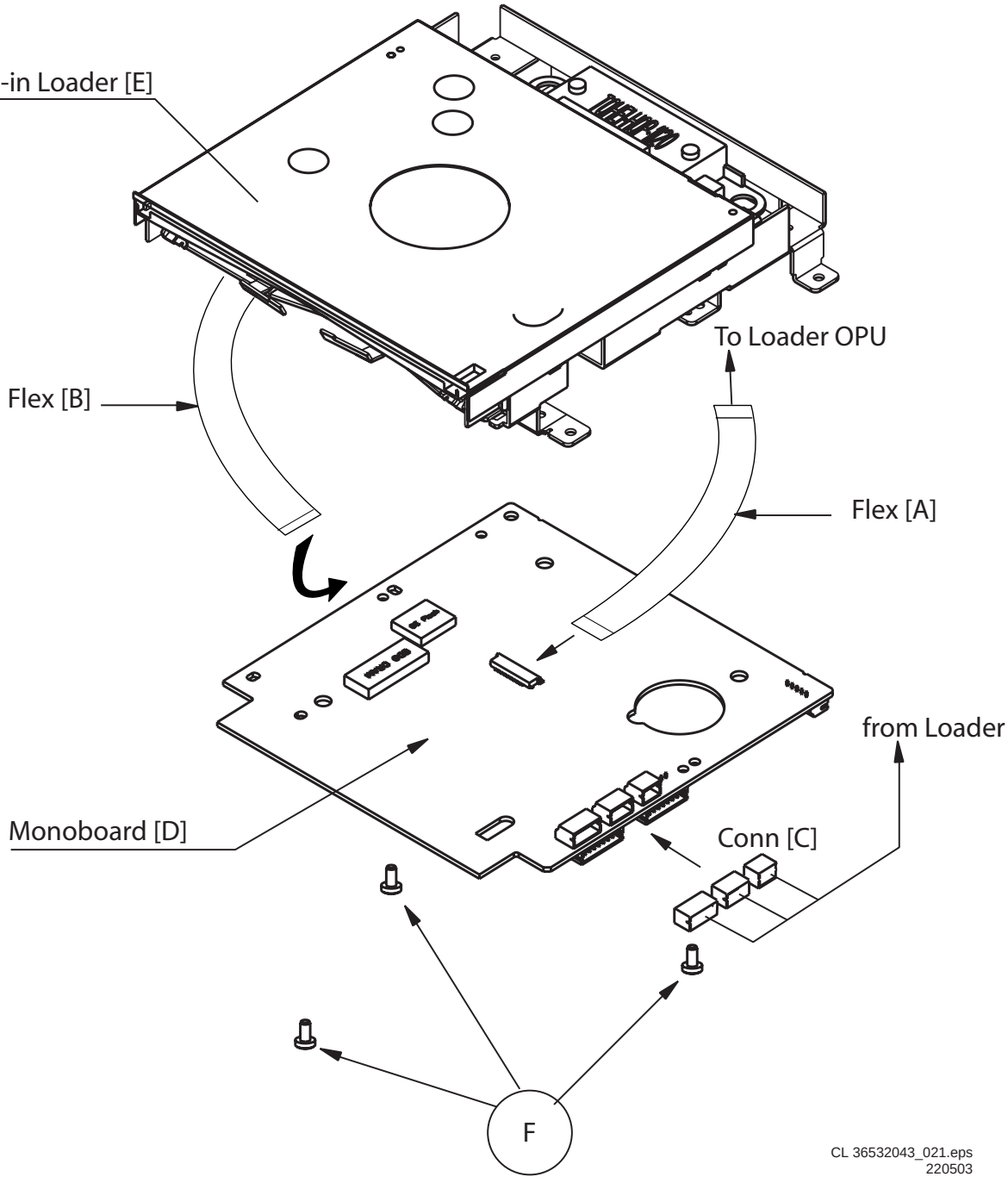


Figure 4-1

4.1.1 Manually Eject the Disc

See Figure 4-2 eject the disc manually.

1. Remove screw,
2. Slide top cover backward,
3. Flip top cover and remove it,
4. Turn the belt in the anti-clockwise direction with your thumb till the disc is ejected,
5. Gently pull the disc out.

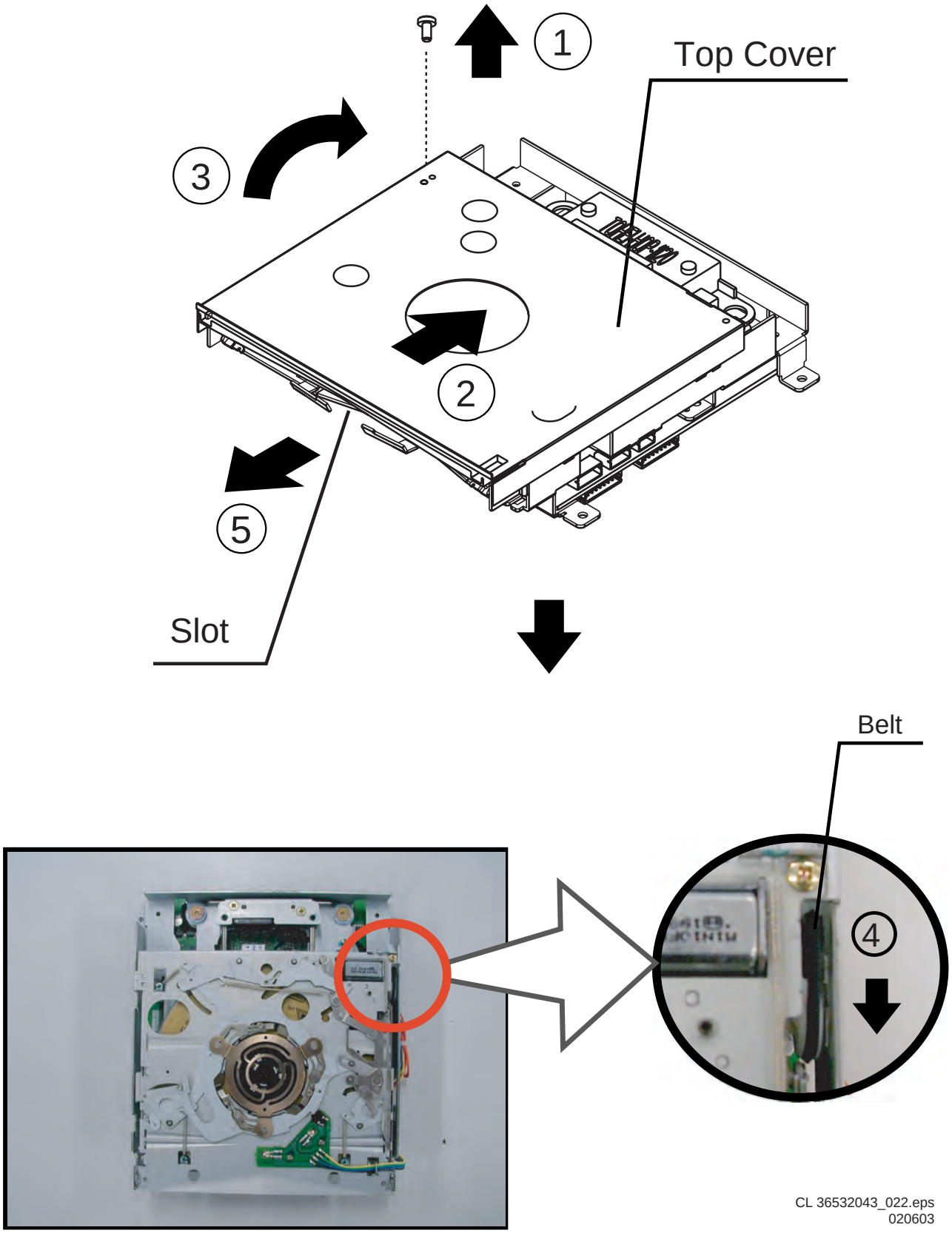


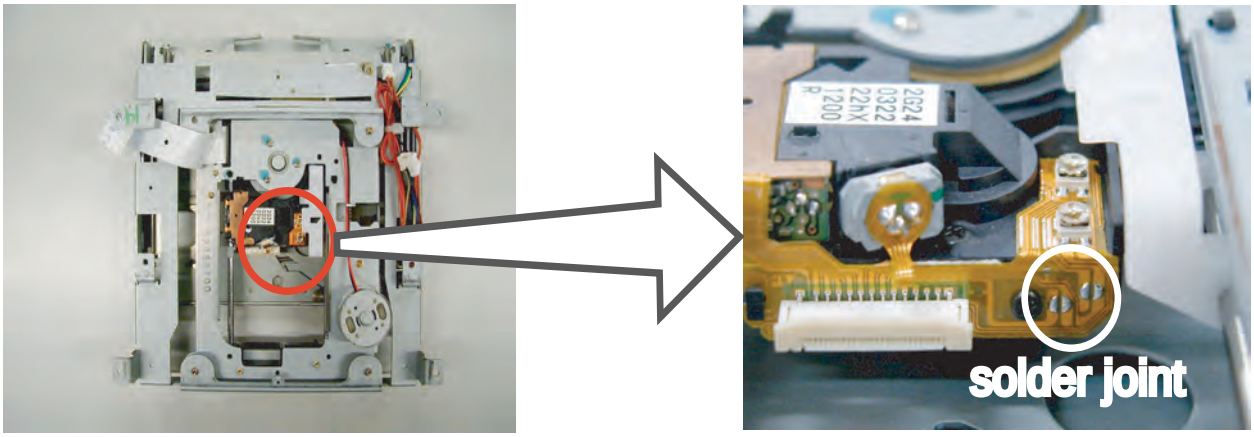
Figure 4-2 Manually eject the disk

4.2 Service Hints

4.2.1 Repair tips

DVD Module SD5.31SL
The DVD module is an integrated unit of TOHEI SLOT-IN loader and Monoboard.

TOHEI SLOT-IN Loader
The loader is a non-repairable unit and in case of failure, it has to be replaced with a new loader.
When replacing with a new Slot-in loader, two solder joints have to be removed after connecting the OPU flex foil to the Monoboard. The solder joints which short circuits the laser diodes to ground are for protection against ESD. Refer to Figure "ESD solder joint" for location of solder points.



CL 36532043_018.eps
020603

Figure 4-3 ESD solder joint

Monoboard
The Monoboard has to be repaired down to components level. Repair handling of the Monoboard requires a workshop with sophisticated de-soldering tools.

4.2.2 Change of Slash number setting

The software setting can be change according to the following procedure:
1. Press PLAY< 159>
2. Enter the 8-digit code <2><2><2><0><0><5><0><0> on the remote control.
3. Press PLAY.
4. The change should effect immediately with information indicated on TV screen.

4.2.3 Software upgrade via Download disc

Both the application and servo software can be flashed into the DVD player by means
of a CD-ROM disc. The CD-ROM disc has to be made with a CD writer SW.

Application software
1. Insert the Upgrade disc into the player.
2. The upgrading operation will start automatically.
3. Once the upgrading process finishes, the player will automatically eject the disc.
4. Remove the Upgrade disc.
5. The player will be restarted automatically and display on TV screen will show

Servo software
1. First, make the CD-R/CD-RW:-
   - Disc format
     - The disc format must be CD-ROM Mode 1 and ISO9660 format.
   - Writing mode
     - The volume name (Label) of the disc must be "ALI_CODE" & the file name of the upgrading firmware must be "PS57.BIN". You must put the file as the first item in the disc.Highly recommended to write only this file into the disc & write it in DAO ie. Disc At Once mode.
2. Upgrading procedure
3. Power-on the module.
4. Insert the Upgrading disc. Make sure that this is the first disc that the module sees, otherwise the module will treat it as a general cd-rom disc & not perform the upgrade.
5. The upgrading process takes about 10 secs. & when it finishes, the disc will be ejected.
6. Power sequence the module for the new code to take effect.

4.2.4 Verify setting

To check that the setting has change successfully.

1. Press button on the remote control while disc tray is open.
2. The texts will appear on the TV screen. That is how it looks like.
   - ***Copyright©***
   - ***Philips 2002-03***
   - ***SD5.31-34***
   - ***30May2003***
   - ***15:42***
   - ***22200500***
   - ***A1133***
   - ***C3091***
   - ***100305R3424***

In the texts, the following numbers refer to:

- SD5.31-34 ==> refer to Application software version
- 30May2003 ==> refer to date software was upgraded
- 15:42 ==> refer to time software was upgraded
- 22200500 ==> refer to Slash version
- 100305R3424 ==> refer to servo software version

4.2.5 Test disc

The following test discs are recommended for use to test the playability of the player.

- DVD disc: MPTD CVP 02.18- 12nc 7104 099 91691
- Audio disc (CDDA): Subchassis 8a Test disc- 12nc 7104 099 28362

4.2.6 Ejecting Disc

When ejecting disc is not possible using remote control

- Short circuit test land [F220] to ground when power supplies are still present with assumption the front end is not faulty.
- When above is not possible, ejecting of the disc has to be done manually. Refer to instruction "Manually Ejecting of disc".

4.2.7 ComPair

For assistance with the repair process of the Monoboard, electronic fault finding guidance has been developed. This program is called ComPair. This ComPair program is available on CDROM. The version of the CDROM for repair of the monoboard is V1.3 or higher and can be ordered with codenumber 4822 727 21637. The procedure for registration is explained in the help file of the program and in the CDROM booklet. The cable to connect the Monoboard with a PC can be ordered with codenumber: 3122 785 90017. All the hardware and software requirements of the systems, necessary for working with ComPair, are described on the CDROM

5. Test Instructions Mono Board SD5.31SL

5.1 General

- Impedance of measuring-equipment should be > 1MΩ.
- Most tests have to be done by software commands. Together with the software command you will find a Ref.# nbr. This is the number of the diagnostic nulceus used for this test. More detailed information can be find in the chapter “Diagnostic Nuclei”.
- Levels: Most measurements are digital measurements. The signal levels specification in this document are defined in the chapter Technical Specifications.
- All the waveforms measurement carried out in these test instruction will be base on the testpoint indicated in the Monoboard schematic diagram in the service manual.

5.2 General Start-up Measurements

5.2.1 Supply Check:

Table 5-1 Supply check

No	Testland	Signal Name	DC Voltage (V)		
			Min	Typ	Max
1	F810	+3V3	3.15V	3.30V	3.50V
2	F811	+5V	4.75V	5.00V	5.25V
3	F813	+12V	10.0V	12.0V	13.2V

The monoboard operates in power-off and power-on mode only. There is no standby mode. In power-off mode, the monoboard does not respond to any communication or signals.

Reset is via an internal reset circuit, which are tied to the +3V3 supply. To ensure proper power recycling, the following timing should be observed:

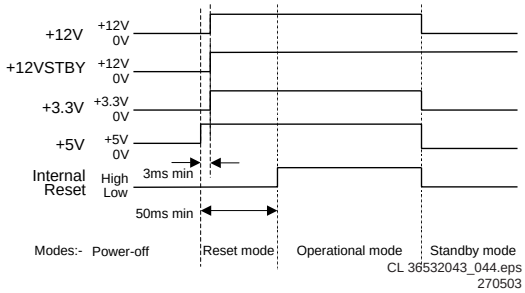


Figure 5-1 Timing chart

All tests that require the diagnostic software should be performed in power-on mode only.

5.2.2 Reset Check:

To ensure a proper start-up of the monoboard, the back-end reset signal SYS_RST is required at the ZIVA-5 input (testpoint F501) after power-on.
To check the reset timing, measure the SYS_RST (testpoint F501) and the +3V3ST supply (testpoint F503), reset circuit trigger signal.

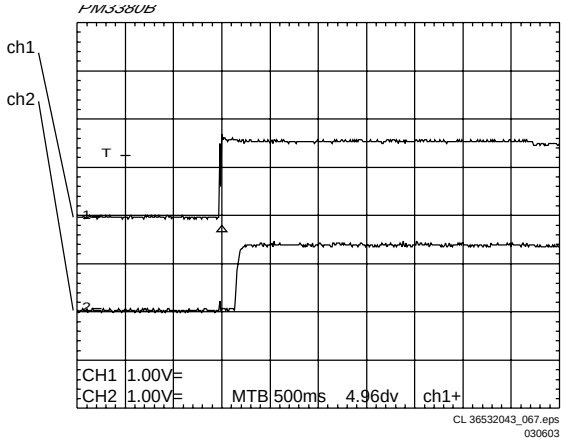


Figure 5-2 Reset

NB: The SYS_RST rising edge,CH2, should be at least 100msec after the +3V3ST (refer to CH1 Figure Reset).
If the reset input does not go high then check the reset circuit around IC7500.

5.2.3 Clock Check

To check the correct functioning of the ZIVA, we first have to check the presence of all clocks.

Table 5-2 Clock check

No	Test land	Signal name	Frequency (MHz)			Descrip-tion
			Min	Typ	Max	
1	F401	XTAL	13.4993	13.5000	13.5007	Back-end clock (± 50ppm)
2	F209	ALI_CLK	33.6994	33.8688	34.0382	Front-end clock (± 0.5%)
3	F421	DA_XCK	18.063	18.432	18.801	Audio clock
4	F502	SD_CLK	119.070	121.500	123.930	SDRAM clock

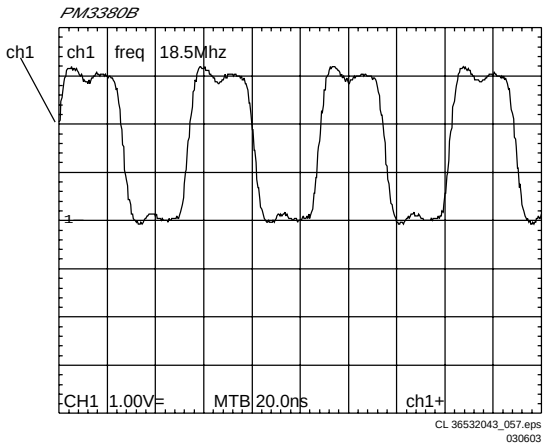


Figure 5-3 DA_XCK

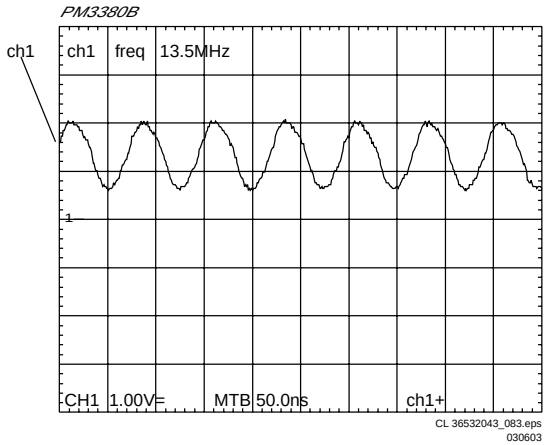


Figure 5-4 XTAL

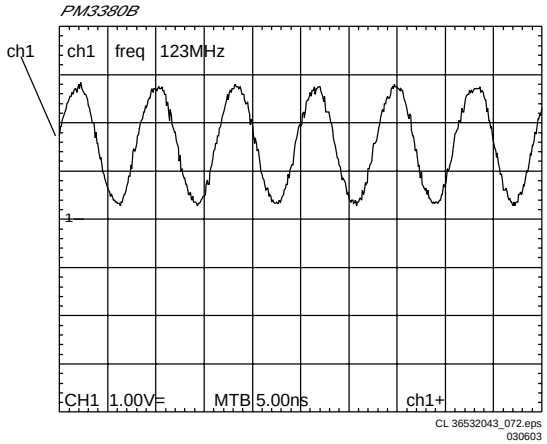


Figure 5-5 SD_CLOCK

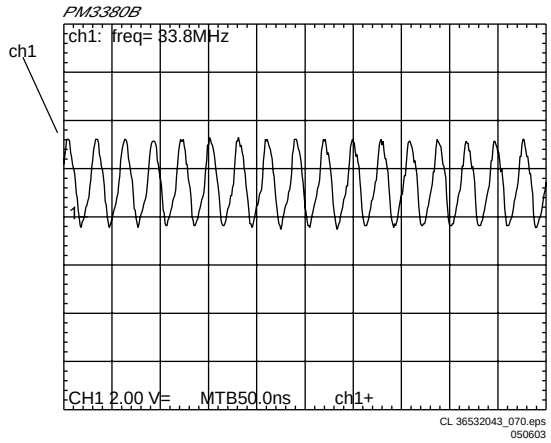


Figure 5-6 ALI_CLOCK

5.3 µP Environment:

5.3.1 General:

All the tests are carried out by diagnostic software. To start the diagnostic software, connect a PC to the serial bus of the ZIVA. Use connector 1702 for this connection.

Table 5-3 PC connection

Connector pin	Signal
1702-1	TXT_SER (service port/UART transmit)
1702-2	SERVICE (service/normal mode select)
1702-3	RXD_SER (service port/UART receive)
1702-4	Not in use
1702-5	GND
1702-6	Not in use
1702-7	+5V_SER

Now start the terminal program. Make sure that the service-pin (pin 1702-2) of the µP is pulled low.
The terminal program of your PC should now display: “DVDv6 Diagnostic software version ...”. This message already means that the µP is running. This is also an indication that the first basic nucleus (nucleus number 1) has been executed during diagnostic start-up. The other commands can be carried out by selecting the “command input” and simply type the reference nbr. to do the test or select the “Menu - driven” test.
To be sure that the µP is able to run the diagnostic software, serial port will be checked during start-up.

Table 5-4 Serial port check

Ref. #	Reference Name	Remark
(1)	BasicSpAcc	Serial port Access test/ initialisation

With this test, the serial communication is checked in both directions.

5.3.2 Memory Check:

The Flash can be check for failure with the PapChksFl command.

Table 5-5 Memory check

Ref. #	Command Name	Remark
6	PapChksFl	Checksum FLASH

The PapChksFl calculate and verify checksum of the FLASH. This includes the entire binary ROM image checksum.

5.4 General I/O Port & Peripherals Check

5.4.1 I2C Bus/NVRAM Check

To access the NVRAM, the I2C bus is used. So by writing and reading to the NVRAM the chip and the bus is checked. With next commands a certain byte is written to the NVRAM. The original information will always be written back into the NVRAM.

Table 5-6 I2C/NVRAM check command

Ref. #	Command Name	Remark
11	PapI2cNvram	I2C NVRAM access

The complete NVRAM can also be checked on failures by writing to all addresses and reading back. This test takes a long time (110 sec).

Table 5-7 NVRAM Write/Read check command

Ref. #	Command Name	Remark
15	PapNvramWrR	NVRAM Write Read

5.4.2 Audio Clock Check

The internally generated Audio clock can be set to either 44.1 kHz (CD_DA), 48 kHz (DVD) or 96 kHZ (DVD). To check the different mode, use the following commands and measure the waveform as correct operation cannot be detected by the Diagnostic Software.

Table 5-8 Audio clock check

Ref #	Command Name	Remark	Test point	Frequency
8a	PapSgsAclk Cdda	Internal PLL CLK in CD-DA mode (Fig 5-4)	F421	16.934 MHz ± 0.02%
8b	PapSgsAclk Dvd	Internal PLL CLK in DVD mode (Fig 5-5)	F421	18.432 MHz ± 0.02%
8c	PapSgsAclk Dvd96	Internal PLL CLK in DVD mode (Fig 5-6)	F421	36.864 MHz ± 0.02%

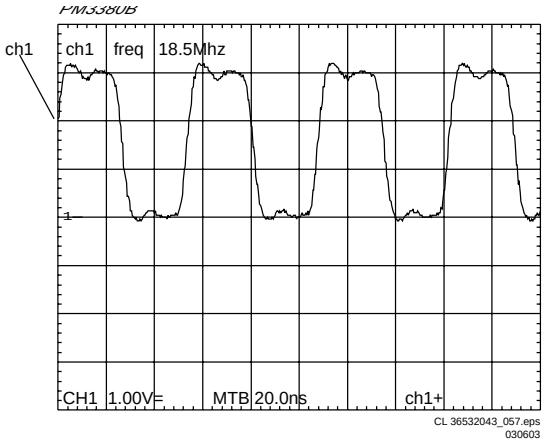


Figure 5-7 Internal PLL CLK in CDDA mode

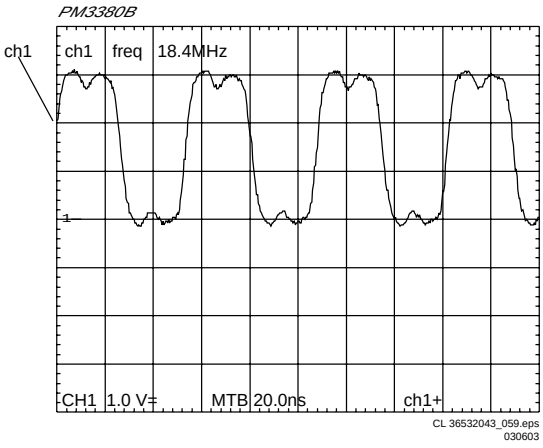


Figure 5-8 Internal PLL CLK in DVD48kHz mode

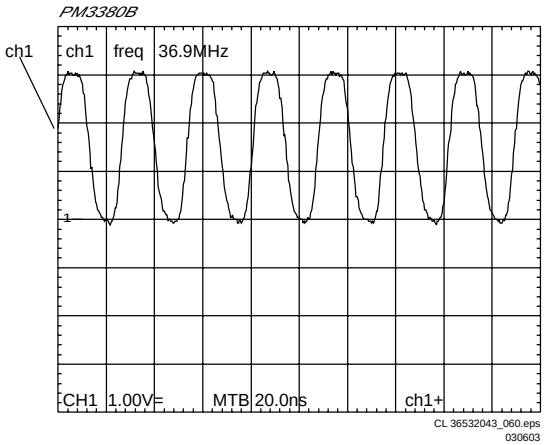


Figure 5-9 Internal PLL CLK in DVD96kHz mode

5.4.3 Audio Mute Check

Switch on the Mute circuit by sending next command:

Table 5-9 Audio mute ON check command

Ref. #	Command Name	Remark
19a	AudioMuteOn	AudioMuteOn

Check the Mute output again at testpoint F603: 3V3 ± 10%
Switch off the Mute circuit by sending next command

Table 5-10 Audio mute OFF check command

Ref. #	Command Name	Remark
19a	AudioMuteOff	AudioMuteOff

Check the Mute output at testpoint F603: 0V ± 0.3V

5.4.4 Audio I2S Check

To check the audio output from the internal audio DAC on the Monoboard, execute the following commands and observe the I2S audio outputs for both sine and pink noise.

Table 5-11 Audio I2S check commands

Ref. #	Command Name	Remark	Audio outputs
21a	AudioSineOn	Audio Sine signal Off	Audio Sine signal On Sine, 1kHz on stereo Press stop button
20a	AudioPinkNoiseOn	Audio Pinknoise On	Pink Noise on 6 channels
20b	AudioPinkNoiseOff	Audio Pinknoise Off	

The audio signal (sine or pink noise) will also be present on the digital ouput (SPDif). This can be checked by connecting an amplifier with digital input.
Check the I2S output.

Table 5-12 NameTestpointWaveform

Name	Testpoint	Description
DA_XCK	F421	Audio clock
DA_BCK	F822	Audio bit clock
DA_DATA0	pin 27/IC7800	Audio data
DA_LRCK	F825	Audio word
SPDIF	F821	Audio digital out

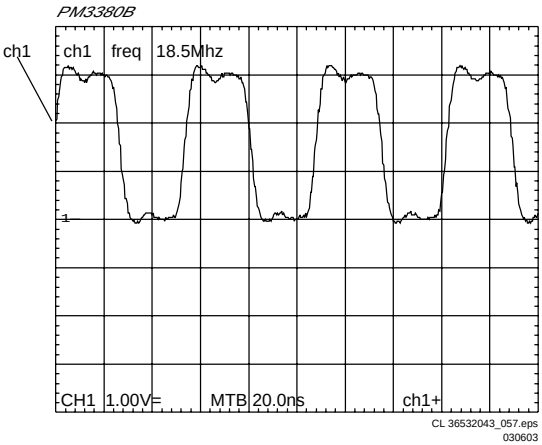


Figure 5-10 DA_XCK

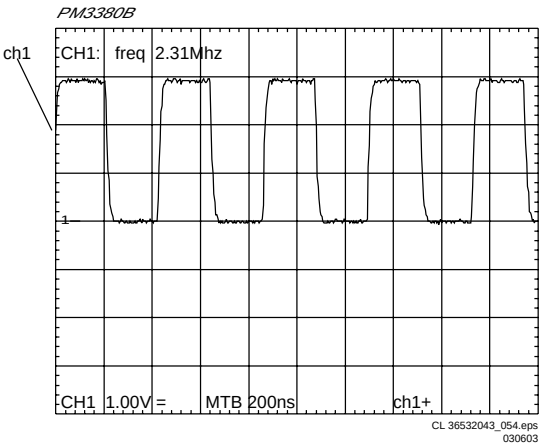


Figure 5-11 DA_BCK

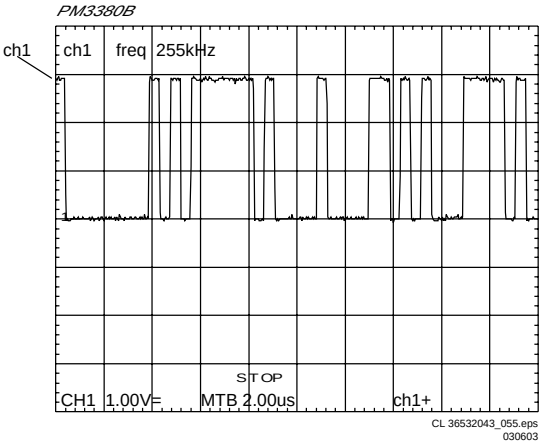


Figure 5-12 DA_DATA0

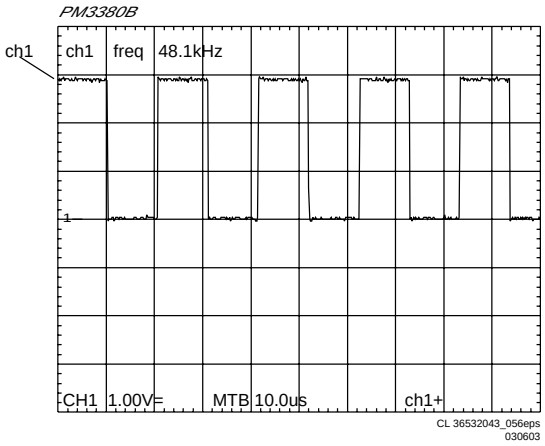


Figure 5-13 DA_LRCK

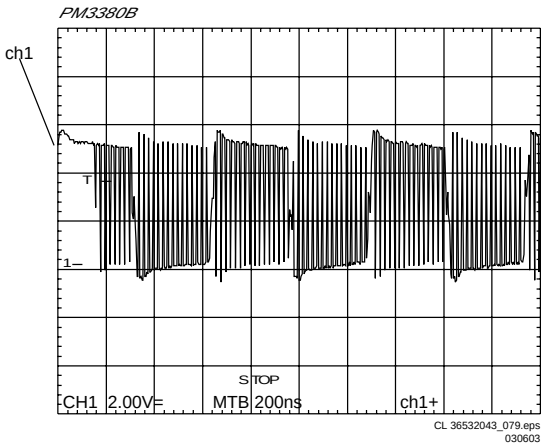


Figure 5-14 SPDIF

To switch the audio signal OFF, press the STOP button on the front.

Without A/V board, the switching levels are as follows:

– DA_DATA1,DA_DATA2 and DA_DATA3 switch between low and high for pink noise. For sine, this is low.
– DA_DATA0, DA_LRCK, DA_XLK and DA_BCK switches between low and high for both pink noise and sine.
– SPDIF switches between LOW and HIGH

5.5 VIDEO

5.5.1 Video Output Check

Measure the DC voltages at all video-outputs at conn 1800 while the video signal is turned off: 1V ± 10%
Generate a color-bar via next software commands:

Ref. #	Command Name	Remark
23a	VideoColDencOn	Colourbar DENC ON
61a	VideoColOutRGB	Set Video out to RGB
61b	VideoColOutYUV	Set Video out to YUV
23b	VideoColDencOff	Colourbar DENC/MPEG OFF

Check video output at the next testpoints:

Name	Testpoint	Waveform
R_V	F817	Refer to Figure R_V
G_Y	F816	Refer to Figure G_Y
B_U	F815	Refer to Figure B_U
C	F819	Refer to Figure C_VIDEO
CVBS	F820	Refer to Figure CVBS_VID

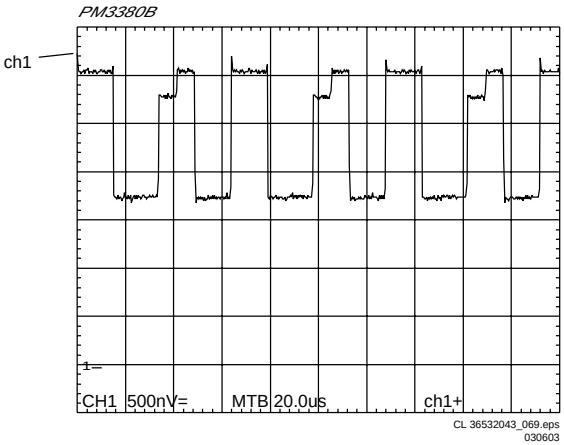


Figure 5-15 R_V with video out at RGB

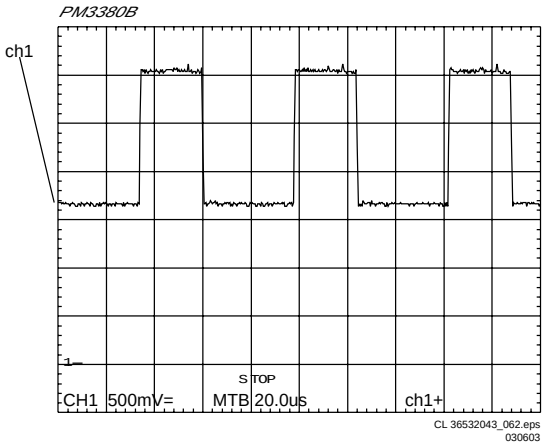


Figure 5-16 G_Y with video out at RGB

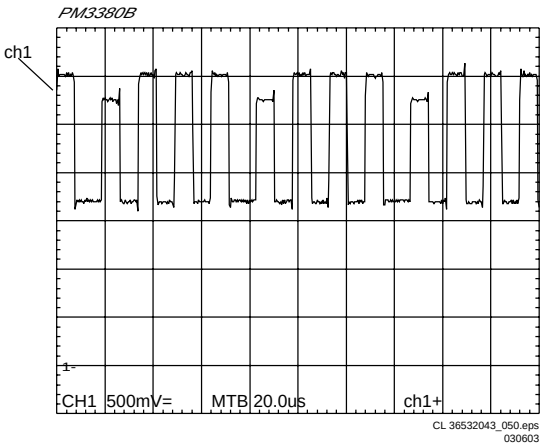


Figure 5-17 B_U with video out at RGB

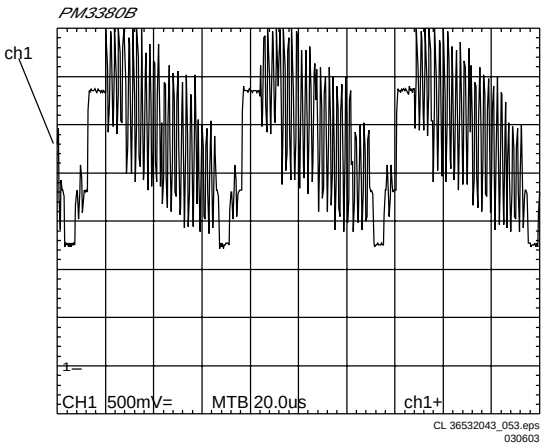


Figure 5-18 CVBS_VID

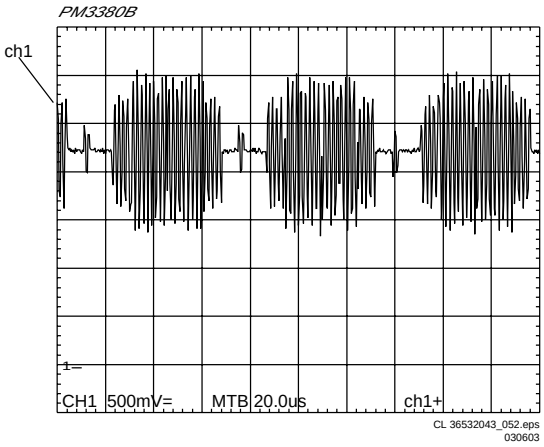


Figure 5-19 C VIDEO

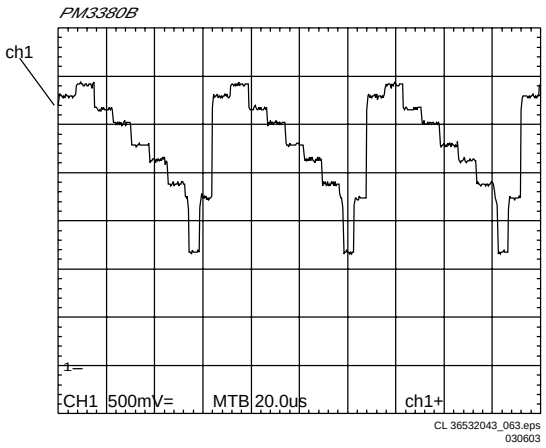


Figure 5-20 G_Y with video out at YUV

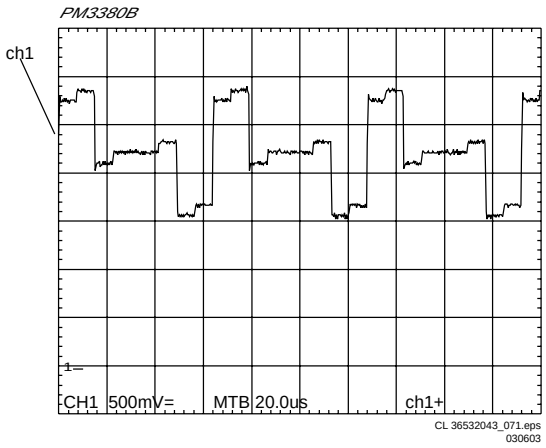


Figure 5-21 R_V with video out at YUV

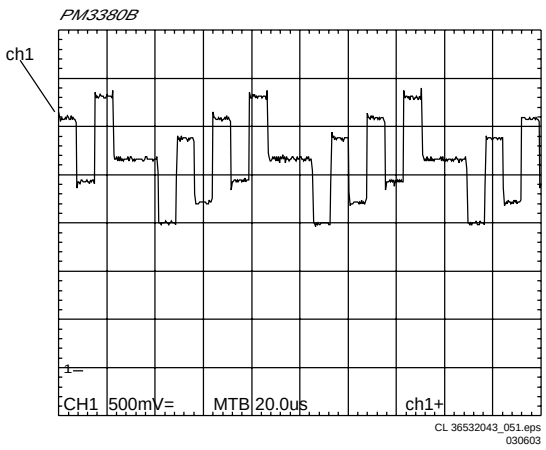


Figure 5-22 B_U with video out at YUV

5.6 Servo

5.6.1 General Start-up Measurements:

Reset the Basic Engine part

Table 5-13 Reset basic engine command

Ref. #	Command Name	Remark
44	BeReset	Reset the Basic Engine

Check the Servo Reset (IDERST) waveform at pin 50 / IC7200 goes from high to low after executing BeReset commands.

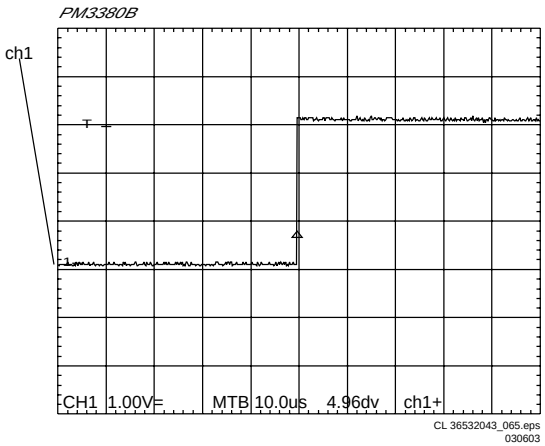


Figure 5-23 IDERST

5.6.2 Spindle Motor check:

The tracking control circuit is checked using the following commands:

Table 5-14 Spindle check commands

Ref. #	Command Name	Remark
39a	BeDiscmotorOn	Discmotor on
39b	BeDiscmotorOff	Discmotor off

Check the following signals with the discmotor switched ON with the loader connected and with DVD Disc inserted.

Table 5-15 Disc motor switching

Signal Name	Testpoint	Frequency
SMOTOR	Pin22/IC7101	Output voltage control
SSPDON	Pin23/IC7101	Power save Motor ON - high Motor OFF - low
VH	Pin15/IC7101	HALL Bias Motor ON - LOW Motor OFF - HIGH
SFGIN	Pin 24/IC7101	Tacho signal output
DA1	F113	Output
DA2	F114	Output
DA3	F115	Output
H1+	F112	H1+ HALL input (positive signal)
H1-	F111	H1- HALL input (negative signal)
H2+	F110	H2+ HALL input (negative signal)
H2-	F109	H2- HALL input (negative signal)
H3+	F108	H3+ HALL input (negative signal)
H3-	F107	H3- HALL input (negative signal)

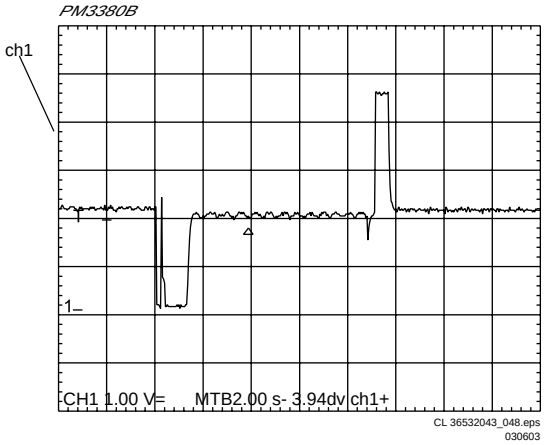


Figure 5-24 SMotor (Random during jump track)

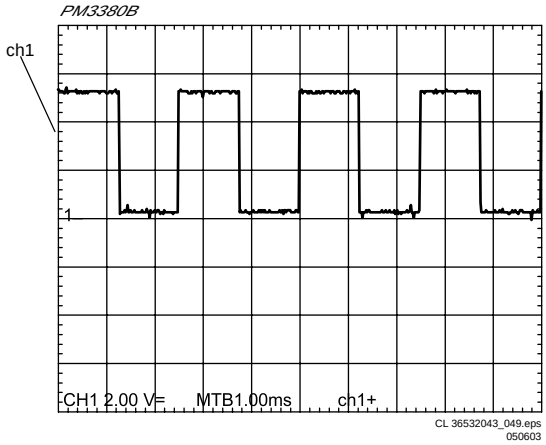


Figure 5-25 SFGIN

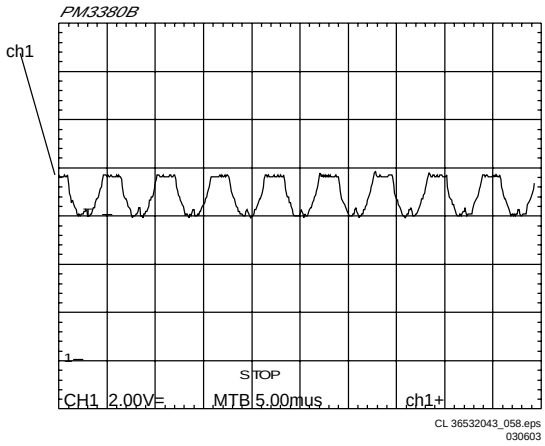


Figure 5-26 DA1-DA2-DA3

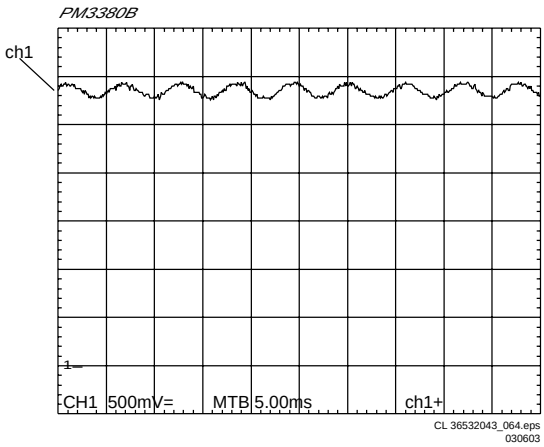


Figure 5-27 HALL input signal

When measurement is completed, switch the discmotor OFF before executing next command

5.6.3 Tracking check

The tracking control circuit is checked using the following commands:

Table 5-16 Tracking

Ref. #	Command Name	Remark
40a	BeRadialOn	Radial control on
40b	BeRadialOff	Radial control off

Visual check on the radial ,when Radial control ON, if the radial movement is visible.
Once the check is completed,switch the Radial control OFF before executing next command

To check the waveform of TRACK- and TRACK+, connect a 10W / 0.25W resistor between TRACK- and TRACK+ to serve as dummy load without connecting the loader.

Table 5-17 Trackingl

Signal Name	Testpoint	Description
Track -	F003	Negative drive to tracking coil
Track +	F004	Positive drive to tracking coil

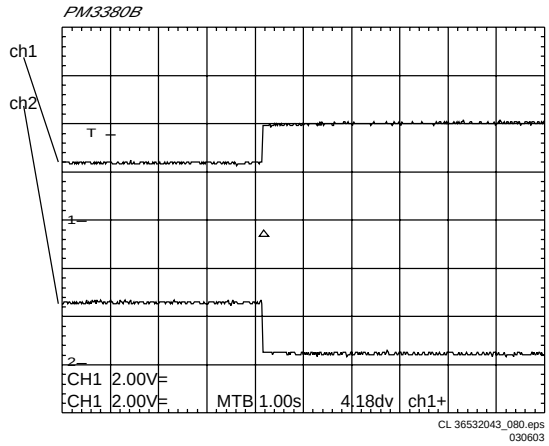


Figure 5-28 TRACK ON Command

5.6.4 Sledge check

The Sledge control circuit is checked using the following commands to move the sledge:

Table 5-18 Sledge check commands

Ref. #	Command Name	Remark
41a	BeSledgeIn	Sledge inwards
41b	BeSledgeOut	Sledge outwards

Visual check on the sledge,when Sledge control ON, if the sledge movement is visible.
Once the check is completed,switch the Sledge control OFF before executing next command

To check the waveform of SLEDGE- and SLEDGE+, connect a 10W / 0.25W resistor between SLEDGE- and SLEDGE+ to serve as dummy load without connecting the loader.

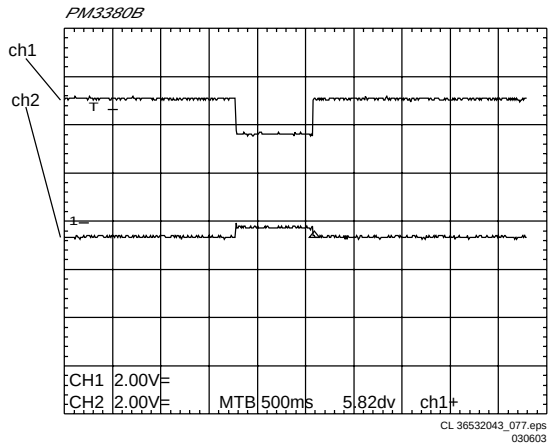


Figure 5-29 SLED Inwards comand

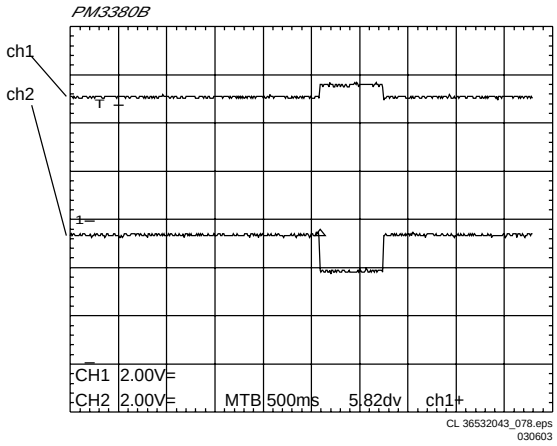


Figure 5-30 SLED Outwards command

5.6.5 Tray Check:

The tray control circuit is checked using the following command:

Table 5-19 Tray command

Ref. #	Command Name	Remark
43a	BeTrayIn	Tray in
43b	BeTrayOut	Tray out

Measure the DC voltages and waveforms when executing the tray closed command.

Table 5-20 Tray in

Signal Name	Testpoint	Value (Tray closed)
LOAD +	F116	2V5 +/- 0V2
LOAD -	F117	2V5 +/- 0V2
INSW	F119	0V +/- 0V2
OUTSW	F121	3V +/- 0V2

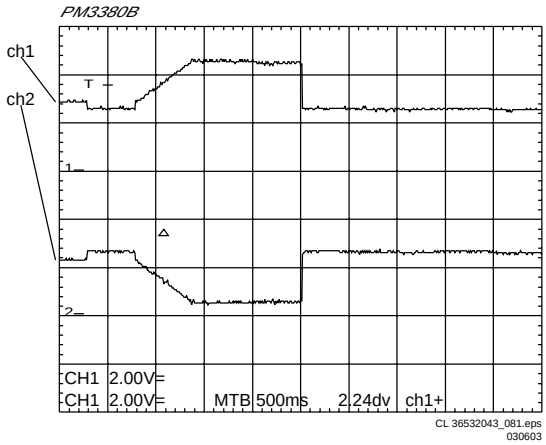


Figure 5-31 Tray in command

Measure the DC voltages and waveforms when executing the tray opening command.

Table 5-21 Tray out

Signal Name	Testpoint	Value (Tray closed)
LOAD +	F116	2V8 ± 0V2
LOAD -	F117	2V2 ± 0V2
INSW	F119	3V ± 0V2
OUTSW	F121	0V ± 0V2

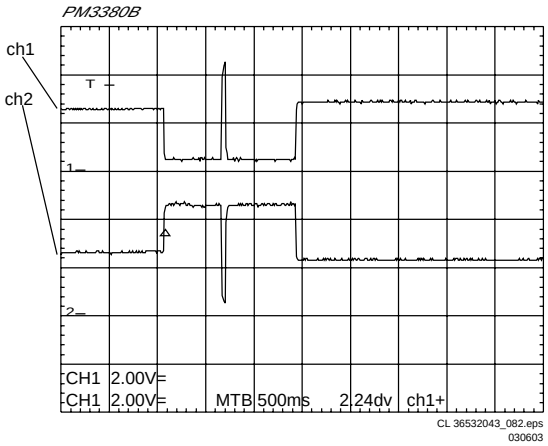


Figure 5-32 Tray out command

5.6.6 Focus check

Test need a DVD disc in the DVD player to operate properly.
The focus control circuit is checked using the following commands:

Table 5-22 Focus check commands

Ref. #	Command Name	Remark
38a	BeFocusOn	Focus on
38b	BefocusOff	Focus off

Visual check on the laser,when Focus control ON, if the laserlight is visible.
Once the check is completed,switch the focus control OFF before executing next command.
To check the waveform of FOCUS- and FOCUS+, connect a 10W / 0.25W resistor between FOCUS- and FOCUS+ to serve as dummy load without connecting the loader.

Table 5-23 Focus motor switching

Signal Name	Testpoint	Description
FOCUS -	F005	Negative drive to focus coil
FOCUS +	F006	Positive drive to focus coil

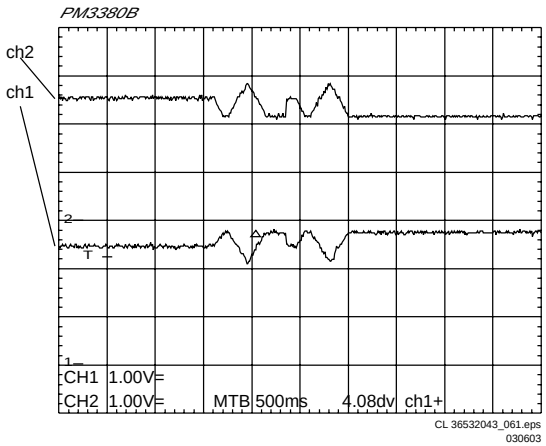


Figure 5-33 Focus ON Command

5.6.7 Hf Path

Play DVD Test Disc.
Measure outputs of diodes A, B, C, D, E, F.

Table 5-24

Signal Name	Testpoint	Value
A	F016	2.5V +/-0.2%
B	F015	2.5V +/-0.2%
C	F014	2.5V +/-0.2%
D	F017	2.5V +/-0.2%
E	F019	2.5V +/-0.2%
F	F018	2.5V +/-0.2%

At outputs of diodes A, B, C, D the following waveform can be measured: Refer to Figure Output of diodes A, B, C, D

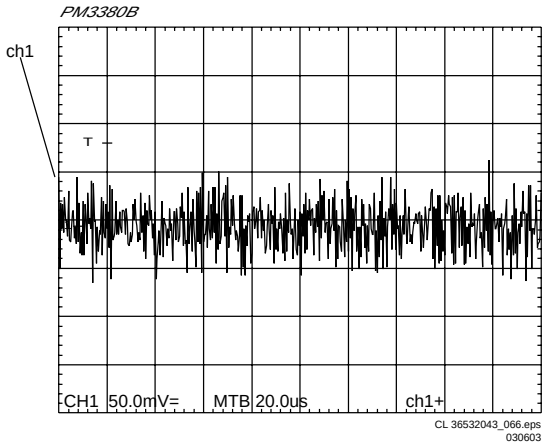


Figure 5-34 Output of diodes A,B,C,D

Check the HF output, RFO, at testland F219 and observe the waveform, refer to Figure RFO.

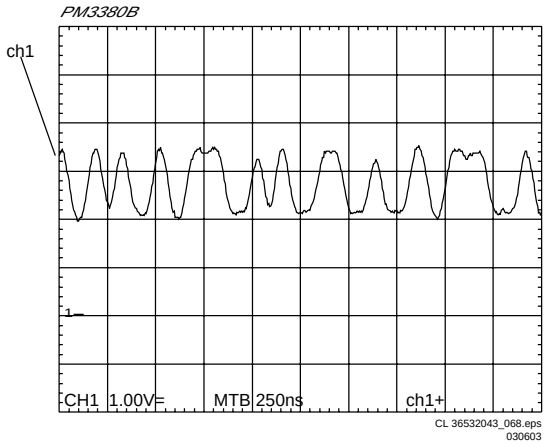


Figure 5-35 RFO

5.7 Diagnostic Software Description

5.7.1 Introduction

Purpose
This document describes all interfaces from the outside world to the diagnostic software, what is needed to use these interfaces and how to access them.

Scope
This document has been realised within the framework of the DVD video player.

5.7.2 Definitions and Abbreviations

Definitions

Control PC	Automatic test equipment, part of the production control system in the factory, to control the execution of Diagnostic Nuclei in the DVD player.
Diagnostic Nucleus	Part of the Diagnostic Software. Each nucleus contains an atomic and software independent diagnostic test, testing a functional part of the DVD player hardware on component level.
Script	Part of the Diagnostic Software. Each script contains a sequence of Diagnostic Nuclei to be executed.
Service PC	PC used by a service- or repair-person to communicate with the Diagnostic Software in the DVD player.

Abbreviations

FDS	Full Diagnostic Software

5.8 Overview of Interfaces

The table below shows an overview of the user interfaces of the Diagnostic Software. The table is based on logical interface, interfaces as seen from user perspective. A logical interface can use one or more physical interface components. The DVD has only a single RS232 port, implying that all interfaces using this port are mutually exclusive.

Table 5-25 Interface overview

Logical Interface	Description	Physical interface components
Menu Interface	Menu-driven activation of individual nuclei, used for Level 2/ Second Line diagnostic mode. Users are service or repair people	- Service PC running a terminal emulation program, connected to the RS232 port of the DVD player. - Test pin grounded
Command Line Interface	Used during Level 1 diagnostic mode. Used to send commands from the Control PC into the DVD hardware.	- Control PC, running a control program (e.g. Hyperterminal), connected to RS232 port of the DVD player. - Test pin grounded

- In the next chapters the logical user interfaces are described in more detail including the exact use of the physical interface components.

5.9 Description of Interfaces

5.9.1 Menu Interface

The menu interface is part of the Level 2 / Second Line diagnostic mode. Via the menu interface it is possible to control the execution of the Diagnostic Nuclei.

Set-up Physical Interface Components
Hardware required:
- Service PC
- one free COM port on the Service PC
- special cable to connect DVD player to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm /Windows Hyperterminal) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD player. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

Activation
Switch the player on and the following text will appear on the screen of the terminal (program):

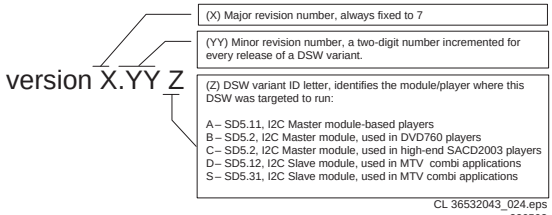
```
DVDv6 Diagnostic Software version 7.03 S

(M)enu, or (C)ommand [M]:@ m <enter>


Press ENTER to go to Main Menu
CC: >
```
CL 36532043_023.eps
020603

Figure 5-36

- The first line indicates that the Diagnostic software has been activated and contains the version number of the diagnostic; this is also an indication that the first basic nucleus (nucleus number 1) has been executed succesfully.
- The term "DVDv6" implies that the DSW is running in the ZiVA5 platform (6th generation).Interpretation of the DSW version is done as follows:



CL 36532043_024.eps
220503

- The second line is the prompt asking the user to choose the interface format. Enter ‘M’ to select Menu mode and the main menu will appear.For the layout of the menus, see chapter ‘Layout of Menu and Submenu’.

To switch between interfaces, the DVD player needs to be switched off and on again.

Note: For player that has no Mechanical power switch, it can be turned on by connecting the power-cable.

Usage
To select, type the number of the chosen menu-item at the prompt. Each entry must be terminated with a ‘RETURN’. Invalid selections will cause an error message by the Menu Handler
Example:

```
Select > 99
Invalid menu choice, number out of range ER @
Press RETURN to continue   @
```
CL 16532163_038.eps
230102

Result and output of an activated (and terminated) nucleus will be sent back to the service terminal.
Example:

```
Select > 3
1301 OK @
Press RETURN to continue   @
```
CL 36532043_025.eps
220503

After the user presses a key, the current menu is rebuilt on screen.
Pressing “RETURN” at the prompt without any further input at the terminal will always rebuild the main menu.

Termination
The menu interface can be terminated by switching off the AC power from the DVD player/ module.

5.9.2 Command Line Interface

The command line interface is part of level 1 diagnostic mode. Via a command line interface the execution of Diagnostic Nuclei can be controlled.

Set-up Physical Interface Components
Hardware required:
- Control PC
- one free COM port on the Control PC
- special cable to connect DVD player to the Control PC

The control PC must use the following port settings for the used COM port: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The control PC is connected with a special cable to the RS232 port of the DVD player. Via the same connection the test pin will be connected to ground.

Activation
After power on the next text will sent to the control PC

```
DVDv6 Diagnostic Software version 7.03 S

(M)enu, OR (C)ommand [M]:@ C <enter>

DD: >
```
CL 36532043_026.eps
220503

The first line indicates that the Diagnostic software has been activated and contains the version number; this is also an indication that the first basic nucleus (nucleus number 1) has been executed succesfully. The second line lets the user choose the interface format. Enter ‘C’ to select Command Mode and the next three lines are the succesful result of the two subsequent basic tests (nuclei 2, 4 and the detection of the display type used by the panel respectively). If not all these messages appear on the terminal screen, then the related nucleus found an error. The last line is the prompt ("DD>"). The diagnostic software is now ready to receive commands.

Note: For player that has no Mechanical power switch, it can be turned on by connecting the power-cable.

Usage
The commands that can be given are the reference IDs of the test nuclei. A command must be terminated with a <RETURN> character from the control PC. When typing commands, the backspace key can be used to make corrections.
In case of typing errors in the command, an error message is returned.
Example:

```
DD: > CompSdarmWrR?       (Nuclei name cannot be accepted)
0001 Unknown command ER @
DD: >
```
CL 16532163_041.eps
230102

If the command (the nucleus ID) is recognised, the nucleus is executed. Result and output of an activated (and terminated) nucleus will be sent back to the control PC according to the standard layout.

Example for a command without error:

```
DD: > 13 <ENTER>      (Execute PapAtapiEcho nuclei)
1300 OK @
DD: >
```
CL 36532043_027.eps
220503

Example for a command with error:

```
DD: > 13 <ENTER>
1304 No response from ATAPI drive ER @
DD: >
```
CL 36532043_028.eps
220503

Termination
The command line interface is terminated by switching off the AC power from the DVD player/ module.

5.10 Layout of Menu and Submenu

5.10.1 Layout Of Menus And Submenus For The Service Terminal

NOTE: a symbol “--” in the menu layouts indicates that that specific menu choice will invoke the display of a submenu. This symbol will also be used in the implementation of the menus (i.e. the “--” will also appear in the user interface).

Menus

MAIN MENU
1 Audio...
2 Video...
3 Front Panel...
4 Basic Engine...
5 Processor Peripherals...
6 Error Log...
7 Miscellaneous...

First Level Submenus

MAIN > AUDIO MENU
1 Mute...
2 Pink Noise...
3 Sine Wave...
4 Digital Ports...

MAIN > VIDEO MENU
1 Colourbar...
2 Digital Port...

MAIN > FRONT PANEL MENU
1 No items available

MAIN > BASIC ENGINE MENU
1 Reset [44]
2 Version [37]
3 ATAPI...
4 Loader Mechanism...
5 Special Diagnostics...

MAIN > PROCESSOR PERIPHERALS MENU
1 Clock...
2 Flash...
3 NVRAM...
4 Processor info [5]
5 Slave IIC Loopback Test [90]

MAIN > ERROR LOG MENU
1 Read Last Errors [31]
2 Read Error Bits [32]
3 Reset Error Log [33]

MAIN > MISCELLANEOUS MENU
1 Statistics Info...
2 Read DVD Application version [46]

Second Level Submenus

MAIN > AUDIO > MUTE MENU
1 Mute On [19a]
2 Mute Off [19b]

MAIN > AUDIO > PINK NOISE MENU
1 Pink Noise On [20a]
2 Pink Noise / Beep Tone Off [20b]
3 Beep Tone On [20c]

MAIN > AUDIO > SINE WAVE MENU
1 Audio Sine On [21a]
2 Audio Burst On [21b]

MAIN > AUDIO > DIGITAL PORTS MENU
1 No test available

MAIN > VIDEO > COLOURBAR MENU
1 Colourbar DENC On (PAL) [23a]
2 Colourbar DENC On (NTSC) [23c]
3 Colourbar DENC/MPEG Off [23b]
4 ProgressiveScan MPEG On [24a]
5 Set Video Out To RGB [61a]
6 Set Video Out To YUV [61b]

MAIN > VIDEO > DIGITAL PORT MENU
1 Video Port Out 0xAA [17a]
2 Video Port Out 0x55 [17b]

MAIN > BASIC ENGINE > ATAPI MENU
1 ATAPI Echo [13]

MAIN > BASIC ENGINE > MECHANISM MENU
1 Disc Motor...
2 Laser...
3 Tray...
4 Focus...
5 Radial...
6 Sledge...
7 Grooves...

MAIN > BASIC ENGINE > SPECIAL DIAGNOSTICS MENU
1 Read FlashID [70]
2 ROM Checksum [71]
3 Scratch Detector Test [72]

MAIN > PROCESSOR PERIPHERALS > PCM CLOCK MENU
1 PCM_CLK In CDDA Mode (11.3MHz) [8a]
2 PCM_CLK In DVD Mode (12.3MHz) [8b]
3 PCM_CLK In DVD96kHz Mode (24.6MHz) [8c]

MAIN > PROCESSOR PERIPHERALS > FLASH MENU
1 Verify FLASH Checksum [6]
2 Show FLASH Checksum [62]
3 FLASH Write Acces [10]

MAIN > PROCESSOR PERIPHERALS > NVRAM MENU
1 I2C NVRAM Acces [11]
2 NVRAM Config [34]
3 NVRAM Reset [35]
4 NVRAM Modify [36]
5 NVRAM Read/Wr Test [15]

MAIN > MISCELLANEOUS > STATISTICS INFO MENU
1 Total Nr Of Times Tray Open [47a]
2 Total Time Power On [47b]
3 Total Play-Time CDDA & VCD [47c]
4 Total Play-Time DVD [47d]

Third Level Submenus

MAIN > BASIC ENGINE > MECHANISM > DISC MOTOR MENU
1 Disc Motor On [39a]
2 Disc Motor Off [39b]

MAIN > BASIC ENGINE > MECHANISM > LASER MENU
1 CD Laser On [58a]
2 CD Laser Off [58b]
3 DVD Laser On [58c]
4 DVD Laser Off [58d]

MAIN > BASIC ENGINE > MECHANISM > TRAY MENU
1 Tray Open [43b]
2 Tray Close [43a]

MAIN > BASIC ENGINE > MECHANISM > FOCUS MENU
1 Focus On [38a] (load DVD first)
2 Focus Off [38b]

MAIN > BASIC ENGINE > MECHANISM > RADIAL MENU
1 Radial Control On [40a] (load DVD first)
2 Radial Control Off [40b]

MAIN > BASIC ENGINE > MECHANISM > SLEDGE MENU

1 Sledge Inwards [41a]
2 Sledge Outwards [41b]

MAIN > BASIC ENGINE > MECHANISM > GROOVES (Uses DVD) MENU

1 Jump To Inside Grooves [42a]
2 Jump To Middle Grooves [42b]
3 Jump To Outside Grooves [42c]

Screen Layout With Menus

When menus are used, no specific screen layout can be given: menu information will not be in a special format, except for the layout as mentioned in the previous paragraphs.

A typical menu session can look as follows:

```
DVDv6 Diagnostic Software version 7.03 S


(M)enu, or (C)ommand [M]:@ <enter>

Press ENTER to go to main menu
CC: > <enter>

MAIN MENU

1. Audio ...
2. Video ...
3. Front Panel ...
4. Basic Engine ...
5. Processor Peripherals ...
6. Error Log ...
7. Miscellaneous ...


Select > 4 <enter>

MAIN > BASIC ENGINE MENU

1. Reset [44]
2. Version [37]
3. S2B
4. Loader Mechanism ...
5. Special Diagnostics ...

Press Enter to go to Main Menu

Select > 5 <enter>

MAIN > BASIC ENGINE > SPECIAL DIAGNOSTIC MENU

1. Read flashID [70]
2. ROM checksum [71]
3. Scratsh detector test [72]
Press Enter to go to Main Menu
```

CL 36532043_029.eps
020603

Figure 5-37

Depending on the height of the screen, the text will start scrolling off the top of the screen.

Layout Of Results Diagnostic Nuclei On Control/service Pc

Results returned from a Diagnostic Nucleus to the control/ service PC will have a maximum length of 300 characters and are terminated by a CR character (included in the string length) The result has the following layout
< number >< string > [OK I ER] @< CR >
The use of the "@" enables the Asterix system on the Control PC to parse the output string of each nucleus into a database.

< number > is a 4-digit decimal number padded with leading zeros if its value is less than 4 digits. The first two digits identify the generating nucleus (or goup of nuclei), the latter two digits indicate the error number.

< string > is a text string containing information about the result of the Diagnostic Nucleus.

< number > and < string > are defined in [SDD_DN] in the output sections of each Nucleus.
Examples:

```
1. 0001 Unknown command ER @
2. 3100 OK @
3. 0901 Data line X is not connected to the DRAM ER @
4. Device ID: 0x01
Manufac ID: 0xC2
7000 OK @
```

CL 16532163_045.eps
230102

5.11 Diagnostic Nuclei

Each nucleus contains an atomic and independent diagnostic test, testing a functional part of the DVD player hardware on component level. Each Nucleus returns a result message to its caller. Some tests (e.g. generating a colour bar) can only return an "OK" result. Internal communication will be done via a uniform interface between the diagnostic Engine, Scripts and the Diagnostic Nuclei.
The diagnostic Engine can only operate if a certain (minimal) set of hardware is functioning properly. To test this set of hardware, a set of basic diagnostic nuclei is embedded in the DVD player. Each basic diagnostic nucleus will only test that part of the hardware which is required for execution of the diagnostic Engine, e.g. a RAM test will only test that part of RAM that is used by the diagnostic engine. After the Diagnostic Engine is operational it is possible to do a full RAM diagnostic. All basic diagnostic nuclei start with prefix 'Basic'.
In the overview each Diagnostic Nucleus consists of a reference number, a reference name and remarks. Reference number and name are coupled and one of them is enough for unique identification.

Table 5-26 Basic diagnostic nuclei

Ref. #	Reference Name	Remark
1	BasicSpAcc	Serial port Access test/ initialization
5	CompProcInfo	Display processor specific info (LOR register, Chip Revision)

Table 5-27 Processor and peripherals

Ref. #	Reference Name	Remark
6	PapChksFl	Calculate and Verify Checksum FLASH
7a	PapUclkAclkCdda	External uClock A_CLK in CD-DA mode (SD5.2only)
7b	PapUclkAclkDvd	External uClock A_CLK in DVD mode (SD5.2 only)
7c	PapUclkAclkDvd96	External uClock A_CLK in DVD (96kHz) mode (SD5.2 only)
8a	PapSgsAclkCdda	Internal PLL CLK in CD-DA mode
8b	PapSgsAclkDvd	Internal PLL CLK in DVD mode
8c	PapSgsAclkDvd96	Internal PLL CLK in DVD mode
10	PapFlashWrAcc	Tests Backend flash Write Access function
11	PapI2cNvram	I2C NVRAM access
12	PapI2cDisp	I2C/Sio Bus-Display PWB communication check
13	PapUdeEcho/ PapATAPIEcho	UDE Echo(SD5.2) / ATAPI echo (SD5.12/SD5.31)
14	PapUdePass	Enter UDE Pass-through (SD5.2 only)
15	PapNvramWrR	NVRAM Write Read
62	PapChksSum	Show checksums stored in flash

Table 5-28 Audio

Ref. #	Reference Name	Remark
19a	AudioMuteOn	Audio Mute On
19b	AudioMuteOff	Audio Mute Off
20a	AudioPinkNoiseOn	Audio Pinknoise On
20b	AudioPinkNoiseOff	Audio Pinknoise (or beep tone) Off
20c	AudioBeepToneOn	Audio Beep Tone On
21a	AudioSineOn	Audio Sine signal On/Off
21b	AudioSineBurst	Audio Sine signal Burst

Table 5-29 Audio DAC related (SD5.2 only)

19a	AudioMuteOn	Audio Mute On
65	DAC_I2C	Resets DAC and check I2C communication with DAC
66a	DAC_I2CEnable	Enable I2C communication to AV board
66b	DAC_I2CDisable	Disable I2C communication to AV board
67a	DAC_ClockInternal	Uses internal clock from monoboard for DAC (256fs)
67b	DAC_ClockExternal	Uses external clock for DAC (384fs)
68a	DAC_AudioPreMuteOn	Enable Audio Pre-mute pin
68b	DAC_AudioPreMuteOff	Disable Audio Pre-mute pin
69a	DAC_CenterOn	Enable Center on pin
69b	DAC_CenterOff	Disable Center on pin
79	DAC_Reset	Resets DAC
80a	DAC_ModeCDDA	Sets DAC to CDDA mode
80b	DAC_ModeDVD48	Sets DAC to DVD mode (48kHz)
80c	DAC_ModeDVD96	Sets DAC to DVD mode (96kHz)
80d	DAC_ModeDSD	Sets DAC to DSD mode
81a	DAC_LowPowerStandbyOn	Enable Low Power Standby
81b	DAC_LowPowerStandbyOff	Disable Low Power Standby
82a	DAC_UpsamplingFreq192k	Sets Upsampling frequency to 192kHz
82b	DAC_UpsamplingFreq96k	Sets Upsampling frequency to 96kHz
82c	DAC_UpsamplingOn	Enable upsampling
82d	DAC_UpsamplingOff	Disable upsampling

Table 5-30 Video

Ref. #	Reference Name	Remark
17a	VidPortOutAA	Output the value 0XAA at the Digital Video Interface Port (SD5.2 only)
17b	VidPortOut55	Output the value 0X55 at the Digital Video Interface Port (SD5.2 only)
23a	VideoColDencOnPAL	Colourbar (PAL) DENC On
23b	VideoColDencOff	Colourbar DENC / Digital Video Off
23c	VideoColDencOnNTSC	Colourbar (NTSC) DENC On
24a	VideoProgMPEGon	Progressive - DigitalVideo Colour Bar ON (SD5.2 only)
24b	VideoYuvMPEGon	Enhanced YUV-DigitalVideo Colour Bar
25a	VideoScartLo	Scart Low (SD5.2 only)
25b	VideoScartMi	Scart Medium (SD5.2 only)
25c	VideoScartHi	Scart High (SD5.2 only)
54	VideoScartSwComm	Scart Switch communication (SD5.2 only)
55a	VideoScartSwDvd	Scart Switch Dvd (SD5.2 only)
55b	VideoScartSwPass	Scart Switch Pass-through (SD5.2 only)
57a	VideoScartPinLo	PIO-pins used for Scart-switching
57b	VideoScartPinMi	PIO-pins used for Scart-switching
57c	VideoScartPinHi	PIO-pins used for Scart-switching
61a	VideoColOutRGB	Enable Video Output to RGB
61b	VideoColOutYUV	Enable Video Output to YUV

Table 5-31 Display (slave processor) (SD5.2 only)

Ref. #	Reference Name	Remark
26	DispVer	Version number
27	DispKeyb	Keyboard
28	DispRc	Remote Control
29	DispLed	LEDs
30a	DispDisplay	VFT Display test
30b	DispLCDisplay	LCD Display test
30c	DispLCDBkLight	LCD Backlight test
60	DispP50	P50 loopback test

Table 5-32 Log (Error logging in Nvram)

Ref. #	Reference Name	Remark
31	LogReadErr	Read last Errors
32	LogReadBits	Read errors Bits
33	LogReset	Reset

Table 5-33 Miscellaneous

Ref. #	Reference Name	Remark
34	MiscReadConfig	Read Configuration area from NVRAM
35	MiscNvramReset	NVRAM Reset
36	MiscNvramMod	Modify NVRAM contents
46	MiscApplVer	Read version of application software
47a	MiscTrayOpenNr	Read the number of times the tray opened
47b	MiscPowerOnTime	Read the total time the player's power has been on
47c	MiscPlayTimeCddaVcd	Read the Playtime of CDDA and VCD discs
47d	MiscPlayTimeDvd	Read the Playtime of DVD discs

Table 5-34 Basic engine

Ref. #	Reference Name	Remark
37	BeVer	Version number
38a	BeFocusOn	Focus On
38b	BeFocusOff	Focus Off
39a	BeDiscmotorOn	Discmotor On
39b	BeDiscmotorOff	Discmotor Off
40a	BeRadialOn	Radial control On
40b	BeRadialOff	Radial control Off
41a	BeSledgeIn	Sledge Inwards
41b	BeSledgeOut	Sledge Outwards
42a	BeGroovesIn	jump Grooves to Inside
42b	BeGroovesMid	jump Grooves to Middle
42c	BeGroovesOut	jump Grooves to Outside
43a	BeTrayIn	Tray In
43b	BeTrayOut	Tray Out
44	BeReset	Reset Basic Engine
58a	LaserCdOn	CD Laser on
58b	LaserCdOff	CD Laser off
58c	LaserDvdOn	DVD Laser on
58d	LaserDvdOff	DVD Laser off
70	BedReadFlashID	Read flash memory manufacturer and device ID
71	BedCalcRomChksum	Calculate ROM checksum
72	BedScratchTest	Test scratch detection circuit

Table 5-35 Furore IC (SD5.2 only)

Ref. #	Reference Name	Remark
62	Furore_SdramWrR	Furore SDRAM Write Read test
63	Furore_SdramWrR Fast	Furore SDRAM interconnection test
64	Furore_Id	Furore version ID check
83	Furore_Reset	Furore reset
84a	Furore_High	Sets Furore output pins DSD_PCM0-9 to high
84b	Furore_Low	Sets Furore output pins DSD_PCM0-9 to low

Table 5-36 Karaoke (not available)

Ref. #	Reference Name	Remark
48a	KaraokeModeOff	Switch Karaoke mode off
48b	KaraokeModeOn	Switch Karaoke mode on
49	KaraokeMicInput	Check path from the microphone input to audio output
50a	KaraokeKeyOn	Set Karaoke Key to the maximum level (1200 cent)
50b	KaraokeKeyOff	Set Karaoke Key to flat octave (0 cent)
51a	KaraokeEchoOn	Set Echo Control fuction on
51b	KaraokeEchoOff	Set Echo Control function off

5.12 Nuclei Error Codes

In the following tables the error description of the error codes will be described.

5.12.1 Audio Nuclei

Error code	Error text
1800	Audio Deemp On OK
1820	Audio Deemp Off OK
1880	Audio Deemp Tri OK
1900	Audio mute On OK
1920	Audio mute Off OK
1940	Audio Front LR mute On OK
1960	Audio Front LR mute Off OK
2000	Audio Pinknosie On OK
2001	Audio Pinknoise On DAC fail
2020	Audio Pinknoise Off OK
2040	Audio Beep tone On OK
2041	Audio Beep tone On DAC fail
2100	Audio Sine On OK
2101	Audio Sine On DAC fail
2120	Audio Sine Burst OK
2121	Audio Sine Burst DAC fail
6600	DAC I2C OK
6601	DAC I2C Bus busy
6602	DAC I2C expander
6603	DAC I2C DAC 4362
6620	DAC I2C enable OK
6640	DAC I2C disable OK
6700	DAC Clk internal OK
6701	DAC Clk internal I2C bus busy
6702	DAC Clk internal I2C failed
6720	DAC Clk external OK
6721	DAC Clk external I2Cbus busy
6722	DAC Clk external I2C failed
6800	DAC Audio pre-mute On OK
6801	DAC Audio pre-mute On I2C bus busy
6802	DAC Audio pre-mute On I2C failed
6820	DAC Audio pre-mute Off OK
6821	DAC Audio pre-mute Off I2C bus busy
6822	DAC Audio pre-mute Off I2C failed
6900	DAC Center On OK
6901	DAC Center On I2C bus busy
6902	DAC Center On I2C failed
6920	DAC Center Off OK
6921	DAC Center Off I2C bus busy
6922	DAC Center Off I2C failed
7900	DAC Reset OK
7901	DAC Reset I2C bus busy
7902	DAC Reset I2C expander
8000	DAC Mode CDDA OK
8001	DAC Mode CDDA I2C bus busy
8002	DAC Mode CDDA I2C failed
8020	DAC Mode DVD48 OK
8021	DAC Mode DVD48 I2C bus busy
8022	DAC Mode DVD48 I2C failed
8040	DAC Mode DVD96 OK
8041	DAC Mode DVD96 I2C bus busy
8042	DAC Mode DVD96 I2C failed
8060	DAC Mode DSD OK
8061	DAC Mode DSD I2C bus busy
8062	DAC Mode DSD I2C failed
8100	DAC Low Power Standby On OK
8101	DAC Low Power Standby On I2C bus busy
8102	DAC Low Power Standby On I2C failed

Error code	Error text
8120	DAC Low Power Standby Off OK
8121	DAC Low Power Standby Off I2C bus busy
8122	DAC Low Power Standby Off I2C failed
8200	DAC Upsample 192k OK
8201	DAC Upsample 192k I2C bus busy
8202	DAC Upsample 192k I2C failed
8220	DAC Upsample 96k OK
8221	DAC Upsample 96k I2C bus busy
8222	DAC Upsample 96k I2C failed
8240	DAC UpSample On OK
8241	DAC UpSample On bus busy
8242	DAC UpSample On I2C failed
8260	DAC UpSample Off OK
8261	DAC UpSample Off bus busy
8262	DAC UpSample Off I2C failed

5.12.2 Basic Engine Nuclei

Error code	Error text
3900	Test successful
3901	“Parity error from Basic Engine to Serial”
3902	“Unexpected response from Basic Engine”
3903	“Communication time-out error”
3904	“Basic Engine returned error number 0xXX”
3921	“Parity error from Basic Engine to Serial”
3922	“Unexpected response from Basic Engine”
3923	“Communication time-out error”
3924	“Basic Engine returned error number 0xXX”
3800	Test successful
3801	“Parity error from Basic Engine to Serial”
3802	“Unexpected response from Basic Engine”
3803	“Communication time-out error”
3804	“Basic Engine returned error number 0xXX”
3805	“Focus loop could not be closed”
3820	Test successful
3821	“Parity error from Basic Engine to Serial”
3822	“Unexpected response from Basic Engine”
3823	“Communication time-out error”
3824	“Basic Engine returned error number 0xXX”
4200	Test successful
4201	“Parity error from Basic Engine to Serial”
4202	“Unexpected response from Basic Engine”
4203	“Communication time-out error”
4204	“Basic Engine returned error number 0xXX”
4205	“Sledge could not be moved to home position”
4206	“Focus loop could not be closed”
4207	“Motor not on speed within time-out”
4208	“Radial loop could not be closed”
4209	“PLL could not lock in accessing or tracking state”
4210	“Subcode or sector information could not be read”
4211	“Requested subcode item could not be found”
4212	“TOC could not be read in time”
4213	“Seek could not be performed”
4220	Test successful

Error code	Error text
4221	“Parity error from Basic Engine to Serial”
4222	“Unexpected response from Basic Engine”
4223	“Communication time-out error”
4224	“Basic Engine returned error number 0xXX”
4225	“Sledge could not be moved to home position”
4226	“Focus loop could not be closed”
4227	“Motor not on speed within time-out”
4228	“Radial loop could not be closed”
4229	“PLL could not lock in accessing or tracking state”
4230	“Subcode or sector information could not be read”
4231	“Requested subcode item could not be found”
4232	“TOC could not be read in time”
4233	“Seek could not be performed”
4240	Test successful
4241	“Parity error from Basic Engine to Serial”
4242	“Unexpected response from Basic Engine”
4243	“Communication time-out error”
4244	“Basic Engine returned error number 0xXX”
4245	“Sledge could not be moved to home position”
4246	“Focus loop could not be closed”
4247	“Motor not on speed within time-out”
4248	“Radial loop could not be closed”
4249	“PLL could not lock in accessing or tracking state”
4250	“Subcode or sector information could not be read”
4251	“Requested subcode item could not be found”
4252	“TOC could not be read in time”
4253	“Seek could not be performed”
4000	Test successful
4001	“Parity error from Basic Engine to Serial”
4002	“Unexpected response from Basic Engine”
4003	“Communication time-out error”
4004	“Basic Engine returned error number 0xXX”
4005	“Radial loop could not be closed”
4020	Test successful
4021	“Parity error from Basic Engine to Serial”
4022	“Unexpected response from Basic Engine”
4023	“Communication time-out error”
4024	“Basic Engine returned error number 0xXX”
4400	Test successful
4401	Test successful
4100	Test successful
4101	“Parity error from Basic Engine to Serial”
4102	“Unexpected response from Basic Engine”
4103	“Communication time-out error”
4104	“Basic Engine returned error number XX”
4120	Test successful
4121	“Parity error from Basic Engine to Serial”
4122	“Unexpected response from Basic Engine”
4123	“Communication time-out error”
4124	“Basic Engine returned error number XX”

Error code	Error text
4300	Test successful
4301	“Parity error from Basic Engine to Serial”
4302	“Unexpected response from Basic Engine”
4303	“Communication time-out error”
4304	“Basic Engine returned error number 0xXX”
4320	Test successful
4321	“Parity error from Basic Engine to Serial”
4322	“Unexpected response from Basic Engine”
4323	“Communication time-out error”
4324	“Basic Engine returned error number 0xXX”
3700	“Version: X.Y.Z”
3701	“Parity error from Basic Engine to Serial”
3702	“Unexpected response from Basic Engine”
3703	“Communication time-out error”
3704	“Basic Engine returned error number 0xXX”
5800	Test successful
5820	Test successful
5840	Test successful
5860	Test successful
5801	"Unexpected response from Basic Engine"
7000	"Manuf. ID: <XX>" "Device ID: <YY>"
7001	"Comm Test Failed"
7002	"Load Cmd Failed"
7003	"Load Dat Failed"
7004	"Run Cmd Failed"
7100	"ROM Checksum: XXXX"
7101	"Comm Test Failed"
7102	"Load Cmd Failed"
7103	"Load Dat Failed"
7104	"Run Cmd Failed"
7201	"Comm Test Failed"
7200	"Test successful"
7202	"Load Cmd Failed"
7203	"Load Dat Failed"
7204	"Run Cmd Failed"
7205	"Scratch circuit not OK"

5.12.3 Display PWB Nuclei

Error code	Error text
3000	“Test successful”
3001	“Disp not responding”
3002	“Disp key no response”
3003	“One or more patterns not correct”
3004	“Disp type invalid”
3020	“Test successful”
3021	“Disp not responding”
3022	“Disp key no response”
3023	“One or more patterns not correct”
3040	“Test successful”
3041	“Disp not responding”
3042	“Disp key no response”
3043	“One or more patterns not correct”
2700	“Model name in wich the test is running”
2701	“Disp key no response”
2702	“Disp not responding”
2707	“Stop key not pressed”
2708	“Pause key not pressed”
2709	“Play key not pressed”
2710	“Open/close key not pressed”
2713	“Previous key not pressed”
2714	“Next key not pressed”
2715	“More than one key not pressed”
2716	" Audio key not pressed"
2900	“Test successful”
2901	“Slave not responding”
2902	“Slave keyboard not responding”
2903	“Standby led not working”
2800	“Test successful”
2801	“Slave display controller not responding”
2802	“Slave keyboard not responding”
2803	“No key press received from remote control”
2600	“The ROM version of the slave processor = 0xXX, and the internal ID = 0xYY”
2601	“I2c bus busy”
2602	“I2c bus not working“
6000	P50 test
6001	“No readback on P50”
6002	“Disp not responding “
6003	“P50 readback error”

5.12.4 Processor & Peripherals Nuclei

Error code	Error text
700	Test successful
720	Test successful
740	Test successful
600	"All checksums are correct"
601	“Following checksum is faulty: BootCode1 Checksum is 0xY2 and is not correct (must be 0xZ2)”
601	“This test is not available when stand-alone compiled”
6200	"Checksums = 0xA1, 0xB1, 0xC1, 0xD1"
6201	“This test is not available when stand-alone compiled”
1000	Test successful
1001	Test successful
1020	Test successful
1021	Test successful
1100	Test successful
1104	“NVRAM reply time-out”
1200	Test successful
1202	“Slave bus not working”
1203	“Slave controller not responding”
1204	“Slave response is not correct”
5900	Test successful

Error code	Error text
5901	“I2c bus busy”
5902	“I2c bus not working“
5904	“DTS chip response not correct”
1300	Test successful
1301	“Parity error from basic engine to serial”
1302	“Parity error from serial to basic engine”
1303	“No communication between serial and basic engine”
1304	“Communication time-out error”
1600	Test successful
1601	“The DVD SDRAM is faulty”

5.12.5 Log Nuclei

Error code	Error text
3100	"Show error log"
3101	"Error log is invalid"
3102	"Error log could not be read from NVRAM"
3103	"I2C bus busy before start"
3200	"Show error bit"
3201	"Error log is invalid"
3202	"I2C bus busy before start"
3203	"Error log could not be read from NVRAM"
3300	"Error log is cleared"
3301	"Error log could not be cleared"
3302	"I2C bus busy before start"

5.12.6 Miscellaneous Nuclei

Error code	Error text
3400	Test successful
3401	“The configuration data could not be read from NVRAM”
3402	“I2C bus busy before start”
3500	“NVRAM is cleared”
3501	“The NVRAM could not be reset.”
3502	“I2C bus busy before start”
3600	“NVRAM contents updated.”
	“NVRAM contents and configuration checksum updated.”
3601	“NVRAM contents could not be updated.”
3602	“I2C bus busy before start”
3603	“NVRAM contents could not be read”
3604	“NVRAM not accessible.”
3605	“NVRAM checksum could not be updated.”
1500	Test successful
1502	“NVRAM access time-out”
1504	“NVRAM fails”
5400	Test successful
5401	“I2c bus busy”
5402	“I2c bus not working“
5403	“Scart switch controller not responding”
5404	“Scart switch controller response not correct”
5500	Test successful
5501	“I2c bus busy”
5502	“I2c bus not working“
5520	Test successful
5521	“I2c bus busy”
5522	“I2c bus not working“
5523	“Scart switch controller not responding”
5200	Test successful
5201	“I2c bus busy”
5202	“I2c bus not working“
5300	Test successful
5301	“I2c bus busy”
5302	“I2c bus not working“
5320	Test successful
5321	“I2c bus busy”
5322	“I2c bus not working“
4700	“Number of times Tray went Open : XX”
4701	The total number of times tray went open could not be read from NVRAM.
4702	I2C bus busy before start
4720	“Total Power On time (minutes) : XX”
4721	The total power-on time could not be read from NVRAM.
4722	I2C bus busy before start
4740	“Total CDDA & VCD disks Play-time (minutes) : XX”
4741	The playtime of CDDA & VCD disks could not be read from NVRAM.
4742	I2C bus busy before start
4760	“Total DVD disks Play-time (minutes) : XX”
4761	The playtime of DVD disks could not be read from NVRAM.
4762	I2C bus busy before start
4600	“Version of Application Software : XX”
4601	“The application version could not be read from NVRAM.”
4602	“I2C bus busy before start”

5.12.7 Video Nuclei

Error code	Error text
1700	Video digital port OK
1701	Video digital port failed
1720	Pscan IO exp OK
1721	Pscan IO exp com failed
2300	Video colourbar On OK
2301	Color Denc On transmit error
2302	I2C Color Denc On bus busy
2320	Video colourbar Off OK
2340	Video colourbar On NTSC OK
2400	ADV7300 com OK
2401	I2C ADV7300 com bus busy
2402	ADV7300 com transit error

Error code	Error text
2403	No ack from ADV7300 com
2404	ADV7300 com response error
2420	FLI2200 com OK
2421	I2C FLI2200 com bus busy
2422	FLI2200 com transmit error
2423	No ack from FLI2200 com
2424	FLI2200 com response error
2460	Proscan com OK
2440	ADV7190 com OK
2441	I2C ADV7190 com bus busy
2442	ADV7190 com transmit error
2443	No ack from ADV7190 com
2444	ADV7190 com response response
2500	Video scart Low OK
2501	I2C Scart Low bus busy
2502	Scart Low transmit error
2520	Video scart Mid OK
2521	I2C Scart Mid bua busy
2522	Scart Mid transmit error
2540	Video scart High OK
2541	I2C Scart High bus busy
2542	Scart High transmit error
6100	Video colour RGB OK
6120	Video colour YUV OK

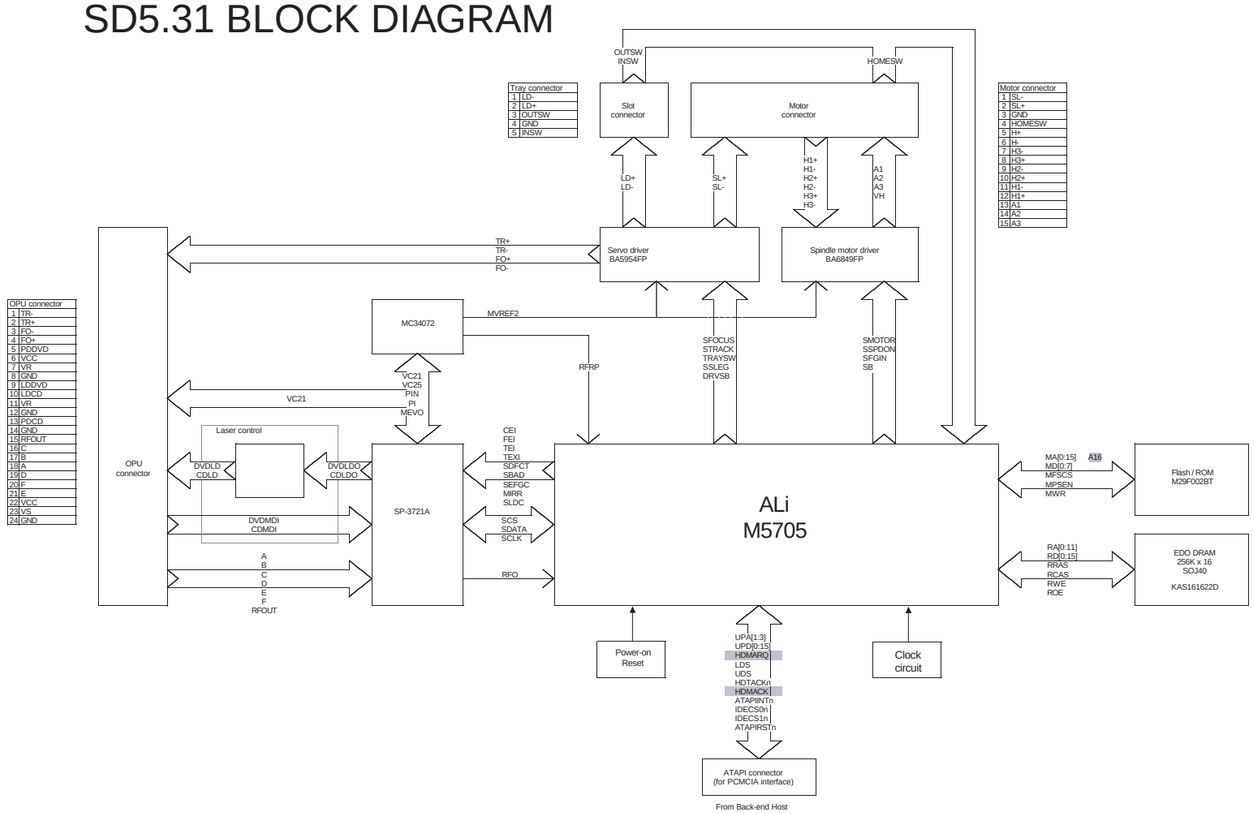
5.12.8 Furore Nuclei

Error code	Error text
6300	Furore Sdram WRR_L OK
6301	Furore Sdram WRR_L DB fail
6302	Furore Sdram WRR_L AB fail
6303	Furore Sdram WRR_L DVC fail
6320	Furore Sdram WRR_H OK
6321	Furore Sdram WRR_H DB fail
6322	Furore Sdram WRR_H AB fail
6323	Furore Sdram WRR_H DVC fail
6400	Furore Sdram WRR_F_L OK
6401	Furore Sdram WRR_F_L DB fail
6402	Furore Sdram WRR_F_L AB fail
6403	Furore Sdram WRR_F_L DVC fail
6420	Furore Sdram WRR_F_H OK
6421	Furore Sdram WRR_F_H DB fail
6422	Furore Sdram WRR_F_H AB fail
6423	Furore Sdram WRR_F_H DVC fail
6500	Furore ID OK
6501	Furore ID invalid
8300	Furore reset OK
8301	Furore reset ID NOK
8400	Furore High OK
8420	Furore Low OK

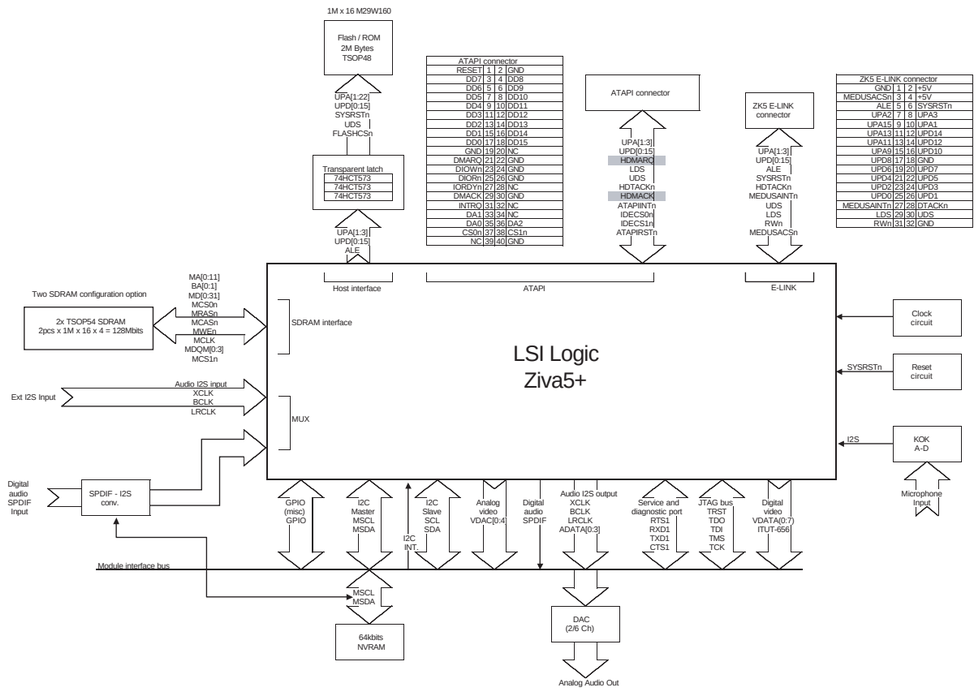
6. Block Diagram and Testpoint Overview Bare Board

Block Diagram

SD5.31 BLOCK DIAGRAM



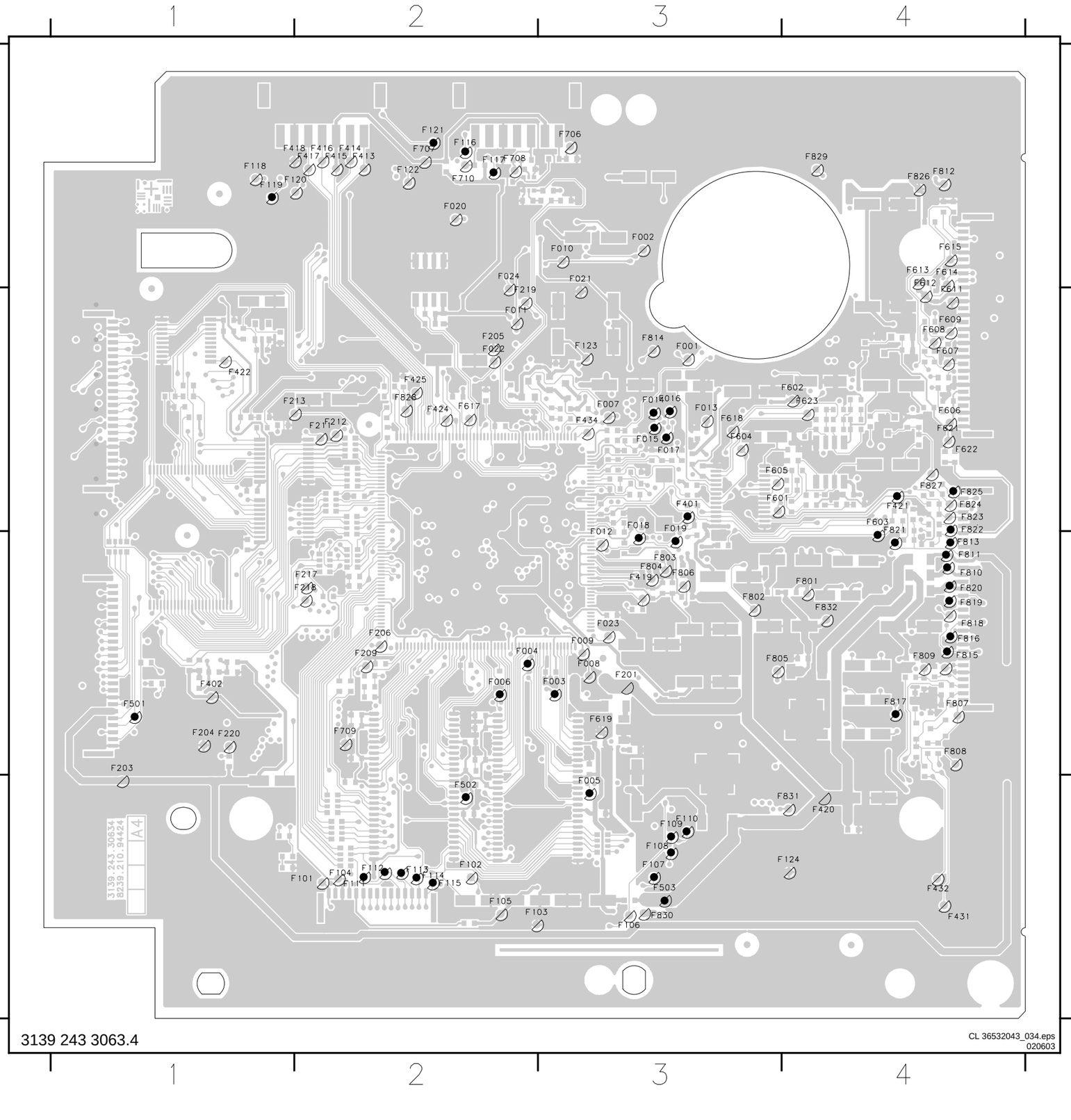
Front-End Engine



Front-End Engine

CL 36532043_043.eps
030603

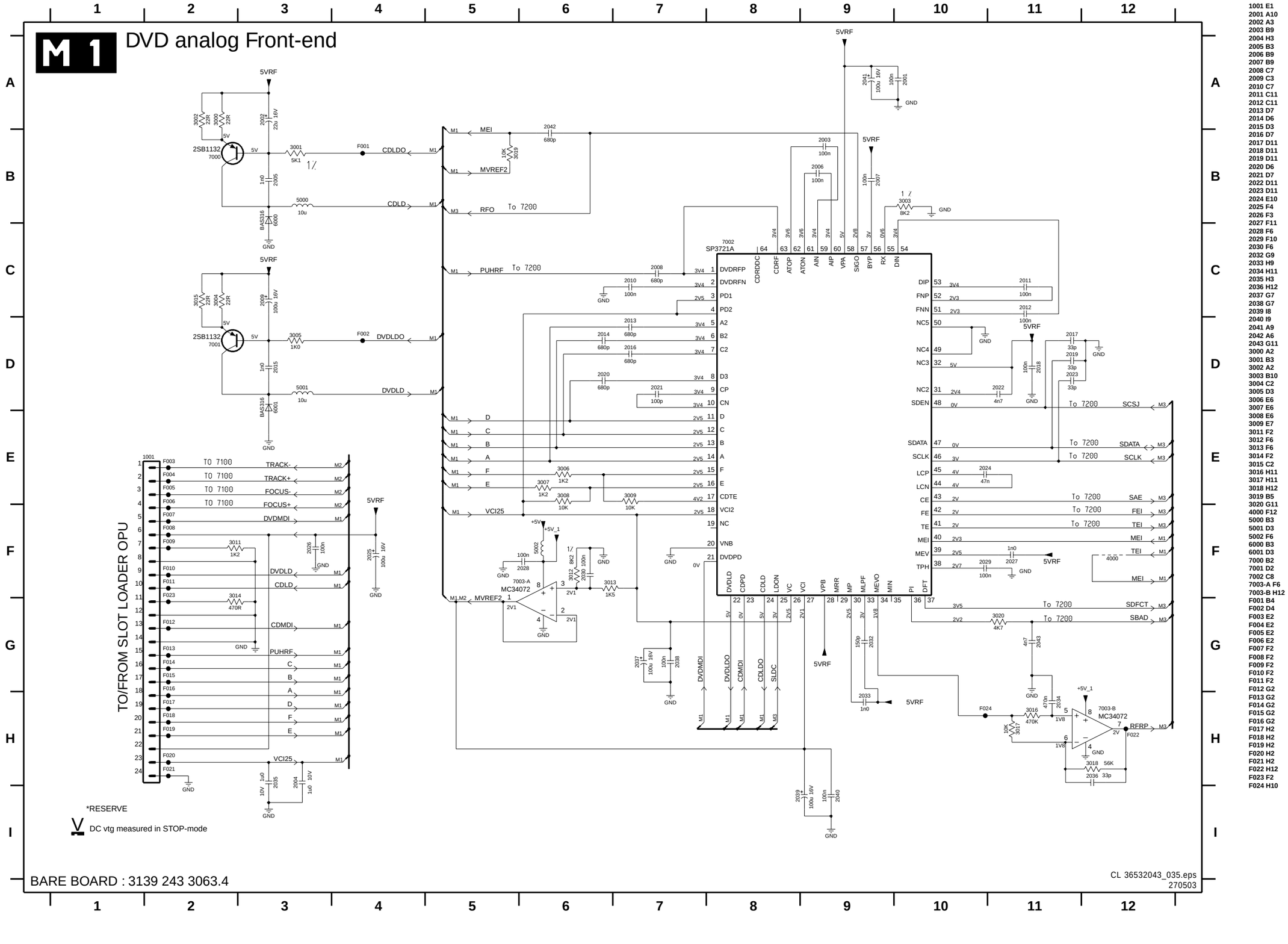
Testpoint Overview Bare Board



F001	B3	F707	A2
F002	A3	F708	A2
F003	C3	F709	C2
F004	C2	F710	A2
F005	D3	F801	C4
F006	C2	F802	C3
F007	B3	F803	C3
F008	C3	F804	C3
F009	C3	F805	C3
F010	A3	F806	C3
F011	B2	F807	C4
F012	C3	F808	C4
F013	B3	F809	C4
F014	B3	F810	C4
F015	B3	F811	C4
F016	B3	F812	A4
F017	B3	F813	C4
F018	C3	F814	B3
F019	C3	F815	C4
F020	A2	F816	C4
F021	B3	F817	C4
F022	B2	F818	C4
F023	C3	F819	C4
F024	B2	F820	C4
F101	D2	F821	C4
F102	D2	F822	C4
F103	D2	F823	B4
F104	D2	F824	B4
F105	D2	F825	B4
F106	D3	F826	A4
F107	D3	F827	B4
F108	D3	F828	B2
F109	D3	F829	A4
F110	D2	F830	D3
F111	D2	F831	D4
F112	D2	F832	C4
F113	D2		
F114	D2		
F115	D2		
F116	A2		
F117	A2		
F118	A1		
F119	A1		
F120	A2		
F121	A2		
F122	A2		
F123	B3		
F124	D4		
F201	C3		
F203	D1		
F204	C1		
F205	B2		
F206	C2		
F209	C2		
F211	B2		
F212	B2		
F213	B1		
F217	C2		
F218	C2		
F219	B2		
F220	C1		
F401	B3		
F402	C1		
F413	A2		
F414	A2		
F415	A2		
F416	A2		
F417	A2		
F418	A1		
F419	C3		
F420	D4		
F421	B4		
F422	B1		
F424	B2		
F425	B2		
F431	D4		
F432	D4		
F434	B3		
F501	C1		
F502	D2		
F503	D3		
F601	B3		
F602	B4		
F603	C4		
F604	B3		
F605	B3		
F606	B4		
F607	B4		
F608	B4		
F609	B4		
F611	B4		
F612	B4		
F613	A4		
F614	A4		
F615	A4		
F617	B2		
F618	B3		
F619	C3		
F621	B4		
F622	B4		
F623	B4		
F706	A3		

7. Electrical Diagrams and PWB's

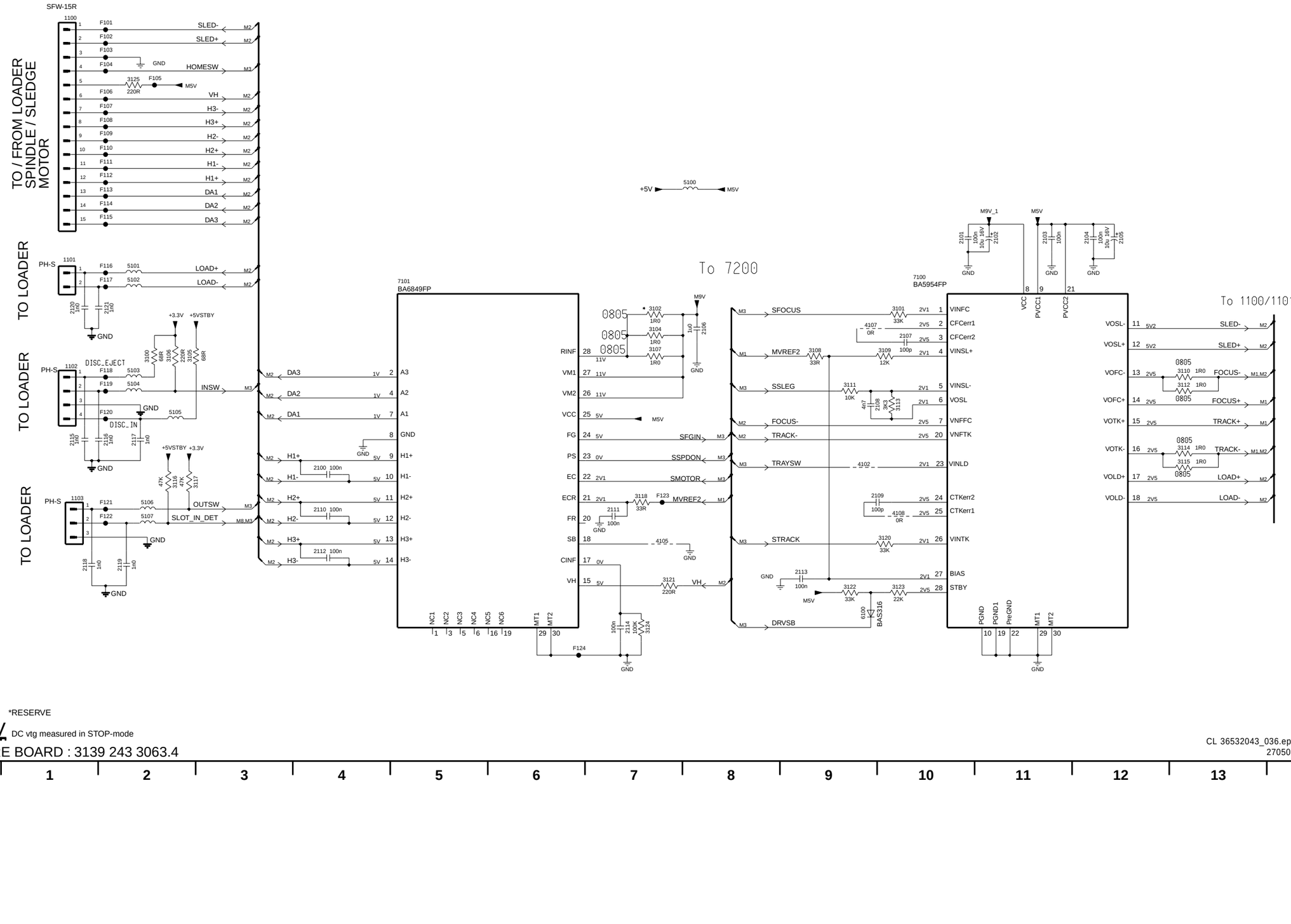
Bare Board: DVD Analog Front-end



1001 E1
2001 A10
2002 A3
2003 B9
2004 H3
2005 B3
2006 B9
2007 B9
2008 C7
2009 C3
2010 C7
2011 C11
2012 C11
2013 D7
2014 D6
2015 D3
2016 D7
2017 D11
2018 D11
2019 D11
2020 D6
2021 D7
2022 D11
2023 D11
2024 E10
2025 F4
2026 F3
2027 F11
2028 F6
2029 F10
2030 F6
2032 G9
2033 H9
2034 H11
2035 H3
2036 H12
2037 G7
2038 G7
2039 I8
2040 I9
2041 A9
2042 A6
2043 G11
3000 A2
3001 B3
3002 A2
3003 B10
3004 C2
3005 D3
3006 E6
3007 E6
3008 E6
3009 E7
3011 F2
3012 F6
3013 F6
3014 F2
3015 C2
3016 H11
3017 H11
3018 H12
3019 B5
3020 G11
4000 F12
5000 B3
5001 D3
5002 F6
6000 B3
6001 D3
7000 B2
7001 D2
7002 C8
7003-A F6
7003-B H12
F001 B4
F002 D4
F003 E2
F004 E2
F005 E2
F006 E2
F007 F2
F008 F2
F009 F2
F010 F2
F011 F2
F012 G2
F013 G2
F014 G2
F015 G2
F016 G2
F017 H2
F018 H2
F019 H2
F020 H2
F021 H2
F022 H12
F023 F2
F024 H10

Bare Board: Spindle/Servo Motor Driver

M2 Spindle / Servo motor driver



*RESERVE

DC vtg measured in STOP-mode

BARE BOARD : 3139 243 3063.4

CL 36532043_036.eps
270503

1100 A1
1101 D1
1102 E1
1103 F1
2100 F4
2101 D10
2102 D11
2103 D11
2104 D12
2105 D12
2106 D8
2107 E10
2108 E9
2109 F10
2110 F4
2111 F7
2112 G4
2113 G9
2114 H7
2115 F1
2116 F2
2117 F2
2118 G1
2119 G2
2120 D1
2121 D2
3100 E2
3101 D10
3102 D7
3104 D7
3105 E2
3106 E2
3107 E7
3108 E9
3109 E10
3110 E13
3111 E9
3112 E13
3113 E10
3114 F13
3115 F13
3116 F2
3117 F2
3118 F7
3120 G10
3121 G7
3122 G9
3123 G10
3124 H7
3125 B2
4102 F9
4105 G7
4107 D9
4108 F10
5100 C8
5101 D2
5102 D2
5103 E2
5104 E2
5105 E2
5106 F2
5107 F2
6100 G9
7100 D10
7101 D5
F101 A2
F102 A2
F103 B2
F104 B2
F105 B2
F106 B2
F107 B2
F108 B2
F109 B2
F110 C2
F111 C2
F112 C2
F113 C2
F114 C2
F115 C2
F116 D2
F117 D2
F118 E2
F119 E2
F120 E2
F121 F2
F122 F2
F123 F7
F124 H6

Bare Board: DVD Front-end Processor

M3 DVD Front-end Processor

*RESERVE

V DC vtg measured in STOP-mode

BARE BOARD : 3139 243 3063.4

CL 36532043_037.eps
020603

1205 I5
2200 A2
2201 A13
2202 A13
2203 A3
2204 A13
2205 B5
2206 B5
2207 B6
2208 B6
2209 B7
2210 B7
2211 C1
2212 C2
2213 C2
2214 C2
2215 B3
2216 B3
2217 B4
2218 B4
2219 B4
2220 B4
2221 B4
2222 D5
2223 D9
2224 D2
2225 F1
2226 F1
2227 F1
2228 F2
2230 F3
2231 F12
2232 E5
2233 G2
2234 G3
2235 G3
2237 H2
2238 H3
2239 I5
2241 I5
3200 D1
3203 B7
3204 B6
3205 B6
3207 B7
3209 B7
3216 C6
3218-1 D10
3218-2 D10
3218-3 D10
3218-4 D10
3220 D2
3224 E2
3225 E2
3226 E2
3227 E2
3228 F5
3229 F3
3231 F5
3232 F5
3233 F2
3234 F5
3235 G2
3236 G2
3238 H2
3239 H3
3240 H2
3241 H11
3242 I2
3243 I11
3244 I5
3245 B10
3247 I12
3248 G5
4203 C5
5200 A2
5201 A12
5202 C1
5203 B3
5204 F12
6201 H3
6202 I2
7200 C6
7201 B12
7202 F12
7203 H2
F201 B3
F203 C1
F204 C3
F205 C2
F206 H3
F209 I6
F211 C8
F212 B7
F213 B7
F217 I7
F218 I7
F219 D4
F220 H5

Bare Board: DVD Back-end Processor

M4 DVD Back-end Processor

TO BACKEND FLASH

JTAG

ZIVA HOST

ZIVA SDRAM

*RESERVE
DC vtg measured in STOP-mode

BARE BOARD : 3139 243 3063.4

CL 36532043_038.eps
020603

1401 B8
1402 F4
2400 A2
2401 A5
2402 A9
2404 A2
2405 A2
2406 A3
2407 A8
2408 A9
2409 A3
2410 B4
2411 B4
2412 B4
2413 B4
2414 B5
2415 B5
2416 B5
2417 B5
2419 C1
2420 D14
2421 D14
2422 D14
2423 D14
2424 F1
2425 E14
2426 G6
2427 F14
2428 H1
2429 F14
2430 F14
2431 F14
2432 F14
2433 F14
2434 G14
2435 G14
2436 G14
2437 G14
2438 A3
2439 E14
3400 B1
3401 C6
3402 D6
3411 B7
3413 B7
3414 B7
3415 B9
3417 B8
3419 B6
3420 B1
3421 B6
3422 B6
3423 C4
3424 B6
3425 B6
3426 C4
3427 B6
3428 B6
3431 D4
3432 C6
3433 C6
3436 E4
3439 E6
3440 F6
3443 G6
3445 G6
3448 H6
3451 H9
3464-1 I8
3464-2 I8
3464-3 I8
3464-4 I8
3465-1 I8
3465-2 I8
3465-3 I8
3465-4 I8
3466-1 I9
3466-2 I8
3466-3 I8
3466-4 I8
3467-1 I9
3467-2 I9
3467-3 I9
3467-4 I9
3468-1 I9
3468-2 I9
3468-3 I9
3468-4 I9
3470-1 I10
3470-2 I10
3470-3 I10
3470-4 I10
3471-1 I10
3471-2 I10
3471-3 I10
3471-4 I10
3472-1 I11
3472-2 I11
3472-3 I10
3472-4 I10
3473 I9
3474-1 H12
3474-2 H12
3474-3 G12
3474-4 G12
3475 G12
3476 G12
3477 G12
3478 B9
3479 F5
3480 A8
4405 I9
4406 C6
4409 B10
4410 C6
4411 C6

Bare Board: Back-end Memory

M5 Back-end Memory

TO M4
ZIVA HOST

VCC3_BEF
7501
980020-48-0237
VCC
UPA(1) 0V 25 A0
UPA(2) 0V 24 A1
UPA(3) 0V 23 A2
UPA(4) 3V 22 A3
UPA(5) 3V 21 A4
UPA(6) 0V 20 A5
UPA(7) 0V 19 A6
UPA(8) 3V 18 A7
UPA(9) 0V 8 A8
UPA(10) 0V 7 A9
UPA(11) 0V 6 A10
UPA(12) 0V 5 A11
UPA(13) 0V 4 A12
UPA(14) 0V 3 A13
UPA(15) 0V 2 A14
UPA(16) 0V 1 A15
UPA(17) 0V 48 A16
UPA(18) 0V 17 A17
UPA(19) 0V 16 A18
UPA(22) 0V 9 A19
UPA(20) 3503 1R0
3502 1R0
DQ0 29 0V UPD(0)
DQ1 31 0V UPD(1)
DQ2 33 0V UPD(2)
DQ3 35 0V UPD(3)
DQ4 38 0V UPD(4)
DQ5 40 0V UPD(5)
DQ6 42 0V UPD(6)
DQ7 44 0V UPD(7)
DQ8 30 0V UPD(8)
DQ9 32 0V UPD(9)
DQ10 34 0V UPD(10)
DQ11 36 0V UPD(11)
DQ12 39 0V UPD(12)
DQ13 41 0V UPD(13)
DQ14 43 0V UPD(14)
DQ15|A-1 45 3V5 UPD(15)
RY|BY_ 15 2V3 3501 1R0 UPA(20)
NC2 10 0V UPA(21)
NC3 13 3504 4K7 VCC3_BEF
NC4 14 3505 4K7 GND
CE_ 26 M4 3V FLASH_CS
OE_ 28 M4 3V R_W
WE_ 11 M4 3V UDS
RESET_ 12 M5 2V6 SYS_RST
BYTE_ 47
VSS1 VSS2 27 46 GND

+3.3V
5500
VCC3_BEF
100n 2502
GND

+3.3V
NCP303
INP OUTP NC RESET CD GND
2 1 4 5 3
2V6
F501
SYS_RST M4,M5,M7
100n 2503
GND
+5V
NC
+5V
4K7 3500
2500 4u7 35V
100n 2504
GND
5502
100n 2513 1R0 3508
GND VCC3_BEF

+3.3V
F503
5501
VCC3_BEM
2505 47u 16V
100n 2506 100n 2507 100n 2508 100n 2509 100n 2510 100n 2511 100n 2512
GND

VCC3_BEM
100n 2514 100n 2515 100n 2516 100n 2517 100n 2518 100n 2519 100n 2520
GND
7502
K4S641632F
49 43 9 3 27 14 1
VDDQ VDD
MDATA(0) 0V8 2 DQ0
MDATA(1) 0V8 4 DQ1
MDATA(2) 0V8 5 DQ2
MDATA(3) 0V8 7 DQ3
MDATA(4) 0V8 8 DQ4
MDATA(5) 1V2 10 DQ5
MDATA(6) 0V8 11 DQ6
MDATA(7) 0V5 13 DQ7
MDATA(8) 0V8 42 DQ8
MDATA(9) 0V8 44 DQ9
MDATA(10) 0V8 45 DQ10
MDATA(11) 0V8 47 DQ11
MDATA(12) 0V8 48 DQ12
MDATA(13) 1V2 50 DQ13
MDATA(14) 1V2 51 DQ14
MDATA(15) 0V8 53 DQ15
OUTPUT BUFFER
LWE
LDQM
I/O CONTROL
DATA INPUT REGISTER
SENSE AMP
1M x 16
1M x 16
1M x 16
1M x 16
ROW DECODER
REFRESH COUNTER ROW BUFFER
ADDRESS REGISTER
BANK SELECT
BA0 20 1V4 BA0
BA1 21 1V4 BA1
A0 23 0V3 MADDR(0)
A1 24 0V3 MADDR(1)
A2 25 0V3 MADDR(2)
A3 26 0V5 MADDR(3)
A4 29 0V5 MADDR(4)
A5 30 0V5 MADDR(5)
A6 31 0V5 MADDR(6)
A7 32 0V5 MADDR(7)
A8 33 0V3 MADDR(8)
A9 34 0V3 MADDR(9)
A10|AP 22 1V6 MADDR(10)
A11 35 0V3 MADDR(11)
COLUMN DECODER
LATENCY & BURST LENGTH
PROGRAMMING REGISTER
COL. BUFFER
LCKE
LRAS
LCBR
LWE
LCAS
LWCBR
TIMING REGISTER
CLK 38 1V6 SD_CLK
CKE 37 VCC3_BEM
3508 1R0 MCS0
CS 19 3V MCS0#
RAS 18 2V8 MRAS
CAS 17 2V8 MCAS
WE 16 3V MWE
UDQM 39 0V2 MDQM1
LDQM 15 0V2 MDQM0
36 NC
40 NC|RFU
VSSQ VSS
52 46 12 6 54 41 28
GND

VCC3_BEM
100n 2514 100n 2515 100n 2516 100n 2517 100n 2518 100n 2519 100n 2520
GND
7503
K4S641632F
49 43 9 3 27 14 1
VDDQ VDD
MDATA(16) 0V8 2 DQ0
MDATA(17) 0V8 4 DQ1
MDATA(18) 0V8 5 DQ2
MDATA(19) 0V8 7 DQ3
MDATA(20) 0V8 8 DQ4
MDATA(21) 0V8 10 DQ5
MDATA(22) 0V5 11 DQ6
MDATA(23) 0V8 13 DQ7
MDATA(24) 0V8 42 DQ8
MDATA(25) 0V8 44 DQ9
MDATA(26) 0V6 45 DQ10
MDATA(27) 0V6 47 DQ11
MDATA(28) 0V9 48 DQ12
MDATA(29) 0V5 50 DQ13
MDATA(30) 0V5 51 DQ14
MDATA(31) 0V9 53 DQ15
OUTPUT BUFFER
LWE
LDQM
I/O CONTROL
DATA INPUT REGISTER
SENSE AMP
1M x 16
1M x 16
1M x 16
1M x 16
ROW DECODER
REFRESH COUNTER ROW BUFFER
ADDRESS REGISTER
BANK SELECT
BA0 20 1V4 BA0
BA1 21 1V4 BA1
A0 23 0V3 MADDR(0)
A1 24 0V3 MADDR(1)
A2 25 0V3 MADDR(2)
A3 26 0V5 MADDR(3)
A4 29 0V5 MADDR(4)
A5 30 0V5 MADDR(5)
A6 31 0V5 MADDR(6)
A7 32 0V5 MADDR(7)
A8 33 0V3 MADDR(8)
A9 34 0V3 MADDR(9)
A10|AP 22 1V6 MADDR(10)
A11 35 0V3 MADDR(11)
COLUMN DECODER
LATENCY & BURST LENGTH
PROGRAMMING REGISTER
COL. BUFFER
LCKE
LRAS
LCBR
LWE
LCAS
LWCBR
TIMING REGISTER
CLK 38 1V6 SD_CLK
CKE 37 VCC3_BEM
CS 19 3V MCS0#
RAS 18 2V8 MRAS
CAS 17 2V8 MCAS
WE 16 3V MWE
UDQM 39 0V2 MDQM3
LDQM 15 0V2 MDQM2
36 NC
40 NC|RFU
VSSQ VSS
52 46 12 6 54 41 28
GND

SD_CLK F502
100R 3507
10p 2521
GND
MCS0#
100R *3510
10p *2522
GND

*RESERVE

DC vtg measured in STOP-mode

TO M4
ZIVA SDRAM INTERFACE

BARE BOARD : 3139 243 3063.4

CL 36532043_039.eps
270503

2500 D5
2502 B11
2503 D6
2504 D5
2505 D10
2506 D11
2507 D11
2508 D11
2509 D11
2510 D11
2511 D11
2512 D11
2513 D6
2514 E3
2515 E3
2516 E3
2517 E4
2518 E4
2519 E4
2520 E4
2521 G13
2522 H13
3500 D5
3501 C8
3502 D7
3503 D6
3504 D8
3505 D9
3506 D7
3507 G13
3508 H4
3510 H13
5500 A11
5501 D10
5502 D6
7500 D5
7501 A7
7502 E4
7503 E11
F501 D5
F502 G13
F503 D11

Bare Board: Audio

M6 Audio

AD1852 (7600)

*RESERVE

DC vtg measured in STOP-mode

BARE BOARD : 3139 243 3063.4

CL 36532043_040.eps
270503

1600 E12
2600 A4
2601 A3
2603 B12
2609 B12
2610 A8
2611 A7
2613 H9
2614 H10
2615 C8
2617 D5
2618 D5
2619 D5
2628 H2
2629 H1
2638 F3
2642 F2
2643 F2
2649 A6
2650 A7
2651 B7
2652 B6
2653 C6
2654 C7
2655 D7
2656 D6
2669 H3
2670 E12
2671 F12
2672 F12
2674 G12
2675 H12
2676 H12
2677 H12
2679 H12
2680 I12
3620 A6
3621 A6
3622 A7
3623 A8
3624 B6
3625 B7
3626 A11
3627 B12
3628 B7
3629 B11
3630 B12
3631 C6
3632 C6
3633 C7
3635 F8
3636 C2
3637 C8
3638 F8
3639 C6
3640 C7
3641 G7
3642 F7
3643 E9
3644 D7
3645 F8
3665 F2
3671 F2
3672 E7
3673 E8
3674 E9
3675 G10
3676 E10
3677 F9
3678 F9
3679 F10
4605 B7
4606 D7
4616 H4
4619 G12
5603 H3
5605 G1
5607 H1
5611 F12
5612 E12
5613 G12
5614 H12
5615 H12
5616 H12
6603 F8
6604 E9
6605 F7
6606 G7
7600 A2
7601 B11
7602-A B7
7602-B C7
7603 B11
7605 G8
7606 F8
7607 F9
7608 E10
7609 G9
7614-A E3
7614-B F3
7615 F10
F601 F3
F602 H3
F603 E6
F604 F6
F605 G6
F606 E12
F607 F12
F608 F12
F609 G12
F611 G11
F612 G12
F613 H12
F614 H12
F615 H12
F617 H12
F618 I12
F619 I11
F621 A10
F622 B10
F623 E3

Bare Board: Services and Debug

M7 Services and Debug

TO 7402 M4

TO 7200 M3

NOT ACTUAL CONNECTOR

*1300

IDE_RST	4712	IDERST	IDERST		1
			GND		2
UPD(9)	3731-D 0R	XHD(1)	XHD(7)		3
UPD(6)	3731-C 0R	XHD(14)	XHD(8)		4
UPD(8)	3731-B 0R	XHD(0)	XHD(6)		5
UPD(7)	3731-A 0R	XHD(15)	XHD(9)		6
UPD(11)	3727-D 0R	XHD(3)	XHD(5)		7
UPD(4)	3727-C 0R	XHD(12)	XHD(10)		8
UPD(10)	3727-B 0R	XHD(2)	XHD(4)		9
UPD(5)	3727-A 0R	XHD(13)	XHD(11)		10
UPD(13)	3728-D 0R	XHD(5)	XHD(3)		11
UPD(2)	3728-C 0R	XHD(10)	XHD(12)		12
UPD(12)	3728-B 0R	XHD(4)	XHD(2)		13
UPD(3)	3728-A 0R	XHD(11)	XHD(13)		14
			XHD(1)		15
			XHD(14)		16
UPD(15)	3732-D 0R	XHD(7)	XHD(0)		17
UPD(0)	3732-C 0R	XHD(8)	XHD(15)		18
UPD(14)	3732-B 0R	XHD(6)			19
UPD(1)	3732-A 0R	XHD(9)			20
			HDRQ		21
LDS	3729-D 0R	IOWJ	IOWJ		22
UDS	3729-C 0R	IORJ			23
DTACK	3729-B 0R	IORDY			24
HIRQ1	3729-A 0R	HINTJ	GND		

+5V — 3735 10K

E-LINK / ATAPI-1

*1301

				GND	1
			IORJ		2
					3
			IORDY		4
				NC	5
			HDACKJ		6
					7
			HINTJ		8
			HCS16J		9
			HA1		10
			HPDIAGJ		11
UPA(2)	3730-D 0R	HA1	HA0		12
UPA(1)	3730-C 0R	HA0	HA2		13
UPA(3)	3730-B 0R	HA2	HCS1J		14
IDE_CS0	3730-A 0R	HCS1J	HCS3J		15
IDE_CS1	4713 0R	HCS3J	HDASPJ		16
				GND	17
			M4 MEDUSA_CS		18
				+5V	19
			M4 ALE		20
			M5 SYS_RST		21
			M4 MEDUSA_INT		22
			M4 R_W		23
				GND	24

4K7 3733, 4K7 3734 → +3.3V

E-LINK / ATAPI-2

SERVICE

1702: 1 TXD_SER, 2 SERVICE, 3 RXD_SER, 4, 5, 6, 7

F706 — 3711 100R — TXD_SER M4

F707 — SERVICE M4

F708 — RXD_SER M4

F709 — GND

F710 — 5704 — +5V

2708 1n5 — GND

+5V — 1K 3710 — 0V

7702-B BC847BS: 3 — 5 0V7 — 4 GND

3700 4K7

3712 4K7 — GND

+5V — 3713 10K — 2V3

7702-A BC847BS: 2 0V — 6 — 1

3714 10K — 3716 6K8 — GND

3717 10K — GND

*RESERVE

DC vtg measured in STOP-mode

BARE BOARD : 3139 243 3063.4

CL 36532043_041.eps
020603

1300 B5
1301 E5
1702 E8
2708 E10
3700 E11
3710 E11
3711 E10
3712 E11
3713 F11
3714 F10
3716 F10
3717 F11
3727-A C2
3727-B C2
3727-C C2
3727-D C2
3728-A D2
3728-B D2
3728-C C2
3728-D C2
3729-A E2
3729-B E2
3729-C E2
3729-D E2
3730-A F2
3730-B F2
3730-C E2
3730-D E2
3731-A B2
3731-B B2
3731-C B2
3731-D B2
3732-A D2
3732-B D2
3732-C D2
3732-D D2
3733 G2
3734 G3
3735 A4
4712 B2
4713 F2
5704 F9
7702-A F11
7702-B E10
F706 E10
F707 E10
F708 F10
F709 F9
F710 F9

Bare Board: Video and Power

M 8 Video and Power

FROM ZIVA

VID_COMP F802 M4 — VID_C F803 M4 — VID_Y F804 M4 — VID_U F805 M4 — VID_V F806 M4

+9V_VID

7800-A BC847BPN — 7800-B BC847BPN
7803-A BC847BPN — 7803-B BC847BPN
7806-A BC847BPN — 7806-B BC847BPN
7809-A BC847BPN — 7809-B BC847BPN
7812-A BC847BPN — 7812-B BC847BPN

ADVANCED AV OUTPUT

M_I2C_CL, S_I2C_CL, M_I2C_DA, S_I2C_DA, I2C_INT, SCART1, SCART0 (FRONT_IRQ), SLOT_IN_DET, MUTE SPDIF, DA_BCK, DA_DATA0 LT, DA_XCK RT, DA_LRCK, MUTE SPDIF, IEC_958

+3.3V — +1.8V — +5V — +12V — +12VSTBY — +5VSTBY — M9V_1 — M9V — +9V

7804 LD1117 — 7814 L78L05ACD — 7807 LF80C — 7810 74HCT1G125

Current using LF90

*RESERVE

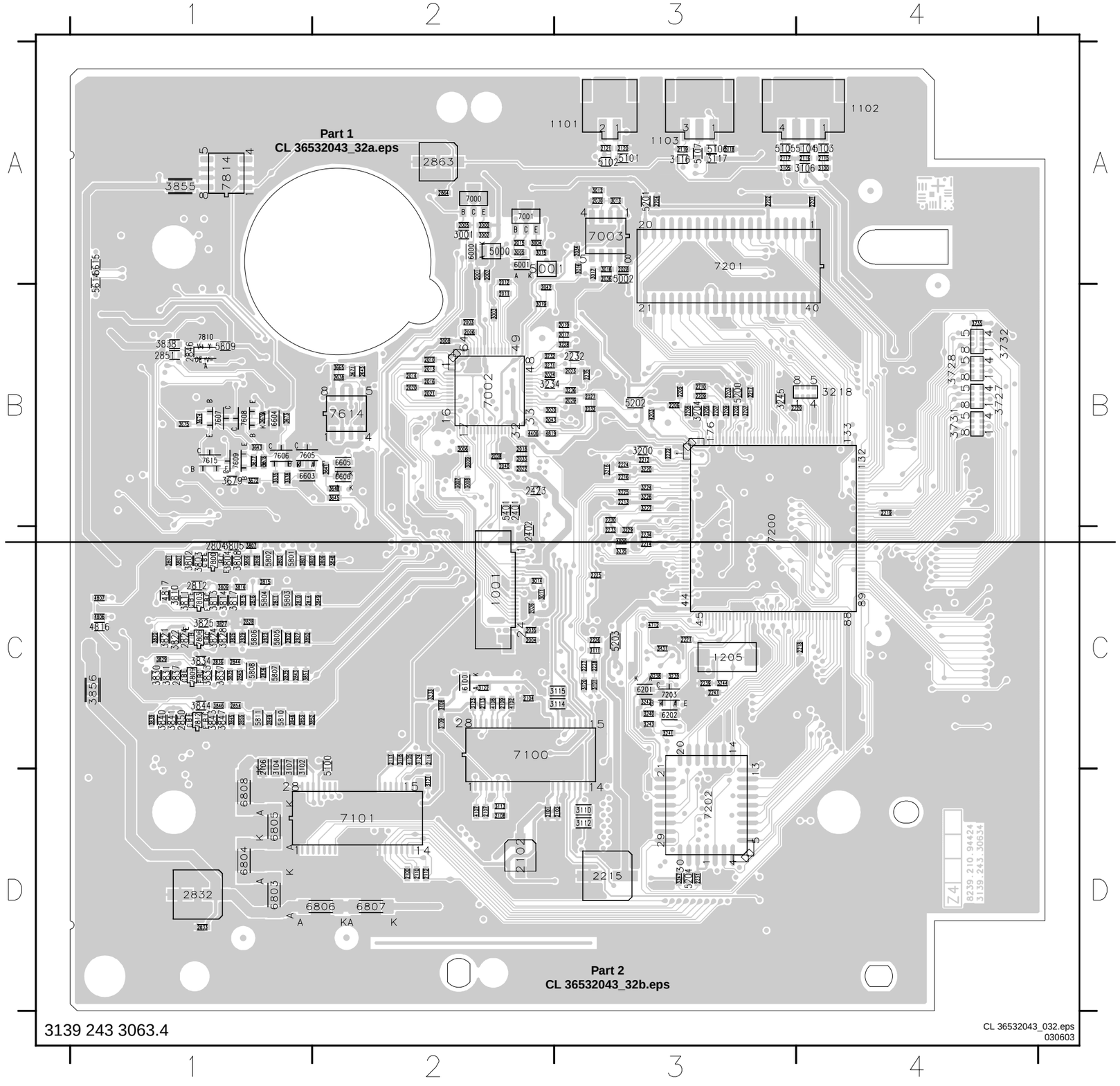
DC vtg measured in STOP-mode

BARE BOARD : 3139 243 3063.4

CL 36532043_042.eps
270503

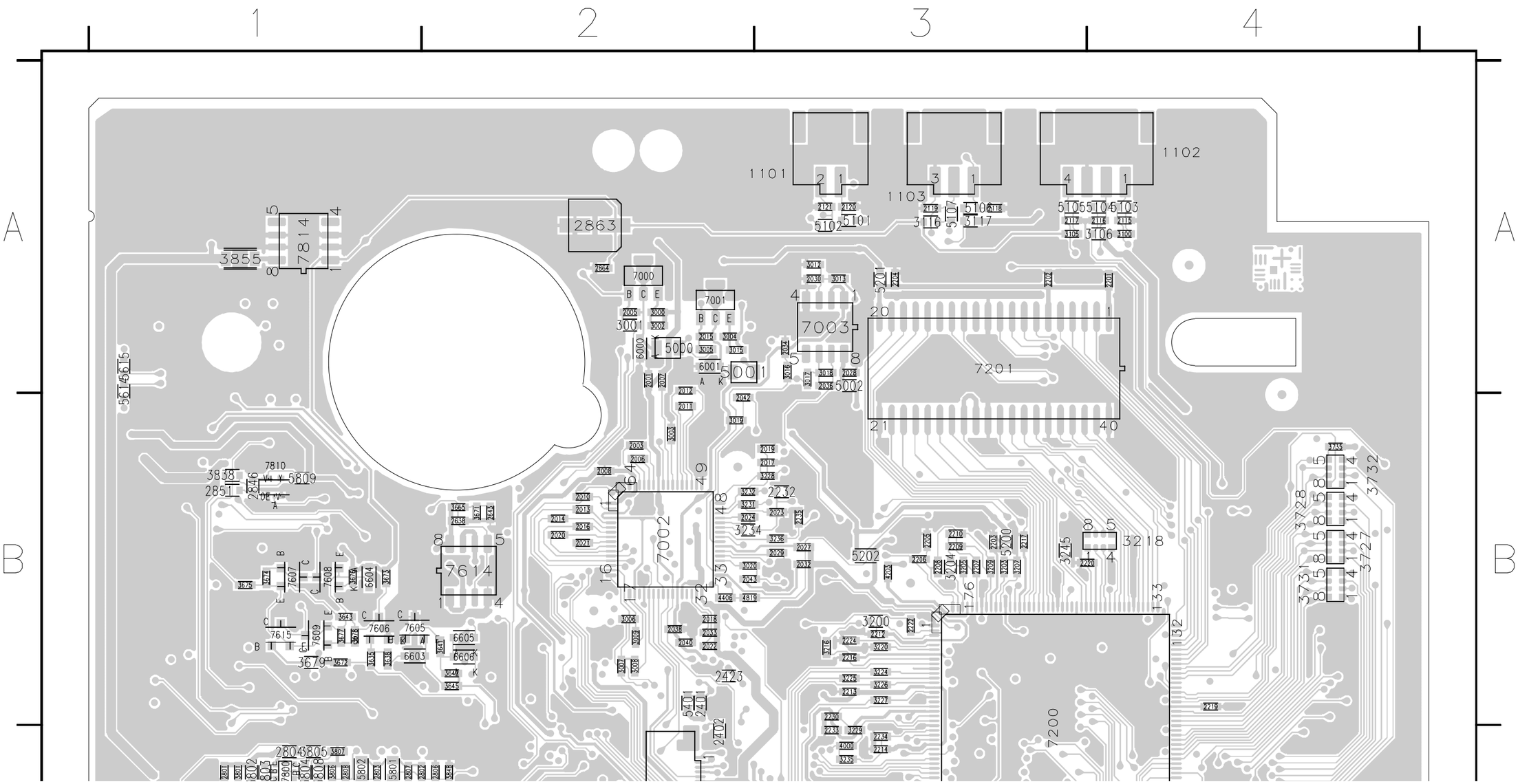
1800 C9	3856 F10
1801 D13	3861 G10
1802 E10	4804 C9
1803 E11	4805 C9
2801 C12	4806 D8
2802 B3	4807 E8
2803 B3	4811 F9
2804 B4	4813 F9
2805 B4	4814 G9
2806 B2	4815 E9
2807 B3	4816 D8
2808 B3	4817 D8
2810 C3	4818 C9
2811 C3	4819 C9
2812 C4	5800 C12
2813 C4	5801 B3
2814 D2	5802 B3
2815 D3	5803 C3
2816 D3	5804 C3
2817 E12	5805 E3
2818 E12	5806 E3
2819 D11	5807 G3
2820 D11	5808 G3
2822 E3	5809 G9
2823 E3	5810 H3
2824 E4	5811 H3
2826 E4	5812 B9
2827 E2	5813 B9
2828 E3	5814 C9
2829 E3	5815 C9
2830 E12	5816 G9
2831 E12	5817 E9
2832 G11	5818 F9
2833 G11	5819 F9
2835 F3	5820 F9
2836 F3	5821 G9
2837 F4	5823 D13
2840 G4	6803 G11
2841 H12	6804 G12
2842 H13	6805 G12
2843 G2	6806 G11
2844 G3	6807 G12
2845 G3	6808 G12
2846 G8	6810 B10
2848 H3	6811 B10
2849 H3	6812 B10
2850 H4	6813 B10
2851 H8	7800-A B5
2852 H4	7800-B B6
2853 H2	7803-A D5
2854 H3	7803-B C6
2855 H3	7804 D12
2856 C10	7806-A E5
2858 F10	7806-B E6
2859 F10	7807 H12
2860 F10	7809-A G5
2861 F10	7809-B F6
2862 F10	7810 H9
2863 F12	7812-A H5
2864 F12	7812-B H6
2865 B9	7814 F11
2866 C10	F801 C12
3801 B4	F802 B2
3802 B5	F803 C2
3803 B5	F804 E2
3804 B5	F805 G2
3805 B6	F806 H2
3806 B3	F807 B9
3807 B4	F808 C9
3808 B4	F809 C9
3809 C4	F810 E10
3810 C5	F811 E11
3811 C5	F812 F11
3813 D5	F813 F10
3814 D6	F814 C9
3815 D3	F815 C9
3816 D4	F816 D9
3817 D4	F817 D9
3820 E4	F818 D9
3821 E5	F819 D9
3822 E5	F820 E9
3824 E5	F821 E9
3825 E6	F822 F9
3826 E3	F823 F9
3827 E4	F824 F9
3828 E4	F825 F9
3829 F4	F826 G10
3830 F5	F827 G9
3831 F5	F828 D13
3833 G5	F829 F12
3834 G6	F830 G12
3835 G3	F831 G13
3836 G4	F832 H13
3837 G4	
3838 H8	
3839 H4	
3840 H5	
3841 H5	
3843 H5	
3844 H6	
3845 H3	
3846 H4	
3847 H4	
3848 B2	
3849 D2	
3850 E2	
3851 G2	
3852 H2	
3855 F11	

Layout Bare Board (Overview Top Side)



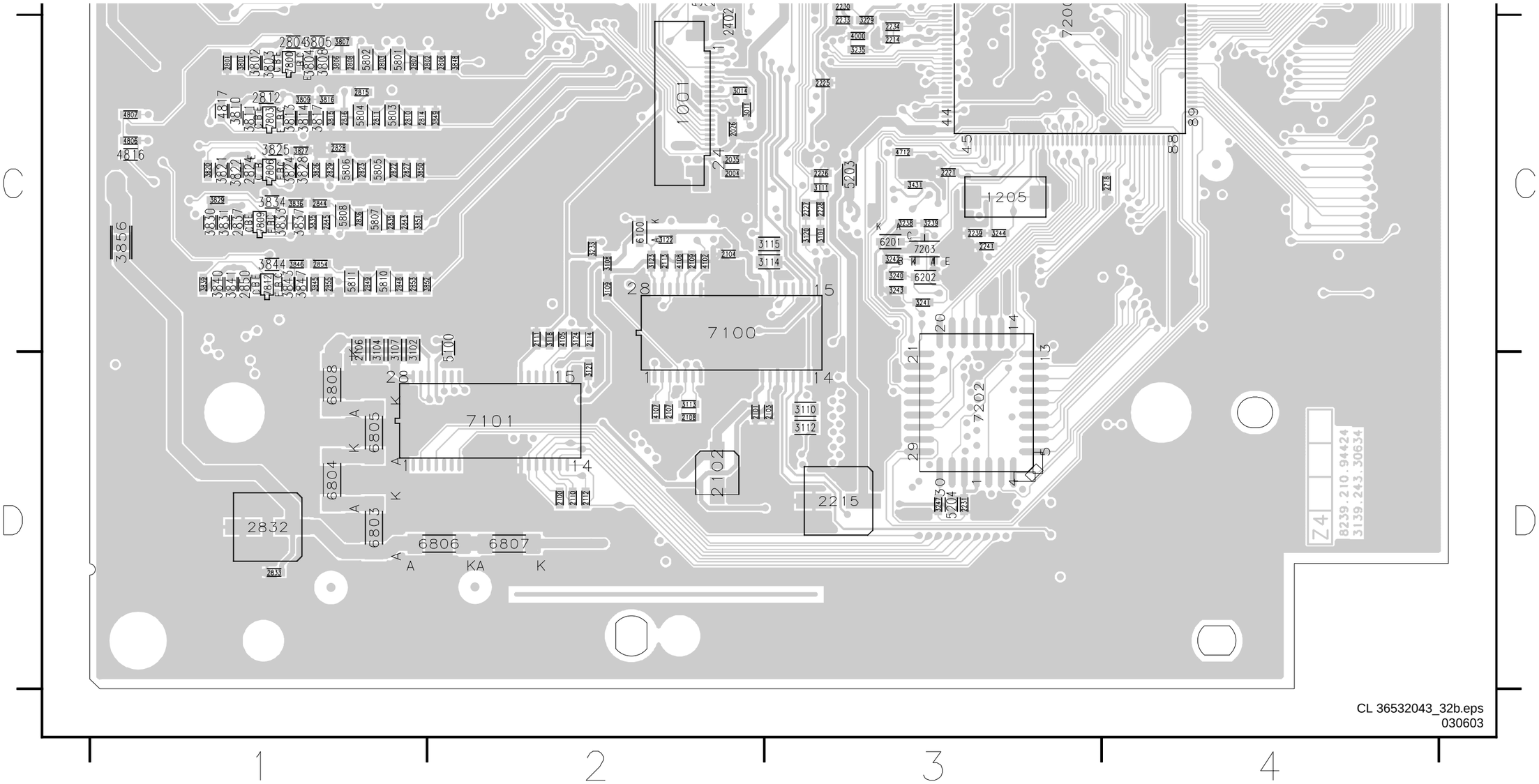
1001	C2	2402	C2	3228	B3	4816	C1
1101	A3	2423	B2	3229	C3	4817	C1
1102	A4	2638	B2	3231	B2	4819	B2
1103	A3	2643	B2	3232	B2	5000	A2
1205	C3	2801	C1	3233	C2	5001	A2
2001	A2	2802	C2	3234	B2	5002	A3
2003	B2	2803	C1	3235	C3	5100	C2
2004	C2	2804	C1	3236	B3	5101	A3
2005	A2	2806	C2	3238	C3	5102	A3
2006	B2	2807	C1	3239	C3	5103	A4
2007	A2	2808	C1	3240	C3	5104	A4
2008	B2	2810	C1	3241	C3	5105	A3
2010	B2	2811	C1	3242	C3	5106	A3
2011	B2	2812	C1	3243	C3	5107	A3
2012	A2	2814	C1	3244	C3	5200	B3
2013	B2	2815	C1	3245	B3	5201	A3
2014	B2	2816	C1	3247	D3	5202	B3
2015	A2	2822	C1	3431	C3	5203	C3
2016	B2	2823	C1	3635	B1	5204	D3
2017	B3	2824	C1	3638	B1	5401	B2
2018	B2	2827	C1	3641	B2	5614	A1
2019	B3	2828	C1	3642	B2	5615	A1
2020	B2	2829	C1	3643	B1	5801	C1
2021	B2	2832	D1	3645	B2	5802	C1
2022	B2	2833	D1	3665	B2	5803	C1
2023	B3	2835	C1	3671	B2	5804	C1
2024	B2	2836	C1	3672	B1	5805	C1
2026	C2	2837	C1	3673	B1	5806	C1
2027	B3	2843	C1	3674	B1	5807	C1
2028	A3	2844	C1	3675	B1	5808	C1
2029	B3	2845	C1	3676	B1	5809	B1
2030	A3	2846	B1	3677	B1	5810	C1
2032	B3	2848	C1	3678	B1	5811	C1
2033	B2	2849	C1	3679	B1	6000	A2
2034	A3	2850	C1	3727	B4	6001	A2
2035	C2	2851	B1	3728	B4	6100	C2
2036	A3	2853	C1	3731	B4	6201	C3
2038	B2	2854	C1	3732	B4	6202	C3
2040	B2	2855	C1	3735	B4	6603	B1
2042	B2	2863	A2	3801	C1	6604	B1
2043	B2	2864	A2	3802	C1	6605	B2
2100	D2	3000	A2	3803	C1	6606	B2
2101	D2	3001	A2	3804	C1	6803	D1
2102	D2	3002	A2	3805	C1	6804	D1
2103	D3	3003	B2	3806	C1	6805	D1
2104	C2	3004	A2	3807	C1	6806	D2
2106	C1	3005	A2	3808	C1	6807	D2
2107	D2	3006	B2	3809	C1	6808	D1
2108	D2	3007	B2	3810	C1	7000	A2
2109	C2	3008	B2	3811	C1	7001	A2
2110	D2	3009	B2	3813	C1	7002	B2
2111	C2	3011	C2	3814	C1	7003	A3
2112	D2	3012	A3	3815	C1	7100	C2
2113	C2	3013	A3	3816	C1	7101	D2
2114	C2	3014	C2	3817	C1	7200	C3
2115	A4	3015	A2	3820	C1	7201	A3
2116	A4	3016	A3	3821	C1	7202	D3
2117	A3	3017	A3	3822	C1	7203	C3
2118	A3	3018	A3	3824	C1	7605	B1
2119	A3	3019	B2	3825	C1	7606	B1
2120	A3	3020	B2	3826	C1	7607	B1
2121	A3	3100	A4	3827	C1	7608	B1
2201	A4	3101	C3	3828	C1	7609	B1
2202	A3	3102	C1	3829	C1	7614	B2
2203	B3	3104	C1	3830	C1	7615	B1
2204	A3	3105	A3	3831	C1	7800	C1
2205	B3	3106	A4	3833	C1	7803	C1
2206	B3	3107	C1	3834	C1	7806	C1
2207	B3	3108	C2	3835	C1	7809	C1
2208	B3	3109	C2	3836	C1	7810	B1
2209	B3	3110	D3	3837	C1	7812	C1
2210	B3	3111	C3	3838	B1	7814	A1
2212	B3	3112	D3	3839	C1		
2213	B3	3113	D2	3840	C1		
2214	C3	3114	C3	3841	C1		
2215	D3	3115	C3	3843	C1		
2216	B3	3116	A3	3844	C1		
2217	B3	3117	A3	3845	C1		
2218	C4	3118	C2	3846	C1		
2219	B4	3120	C3	3847	C1		
2220	B4	3121	D2	3848	C2		
2221	C3	3122	C2	3849	C2		
2222	B3	3123	C2	3850	C1		
2224	B3	3124	C2	3851	C1		
2225	C3	3200	B3	3852	C1		
2226	C3	3203	B3	3855	A1		
2227	C3	3204	B3	3856	C1		
2228	C3	3205	B3	4000	C3		
2230	B3	3207	B3	4102	C2		
2231	D3	3209	B3	4105	C2		
2232	B3	3216	B3	4107	D2		
2233	C3	3218	B4	4108	C2		
2234	C3	3220	B3	4203	B3		
2235	B3	3224	B3	4406	B2		
2239	C3	3225	B3	4712	C3		
2241	C3	3226	B3	4806	C1		
2401	B2	3227	B3	4807	C1		

Layout Bare Board (Part 1 Top Side)

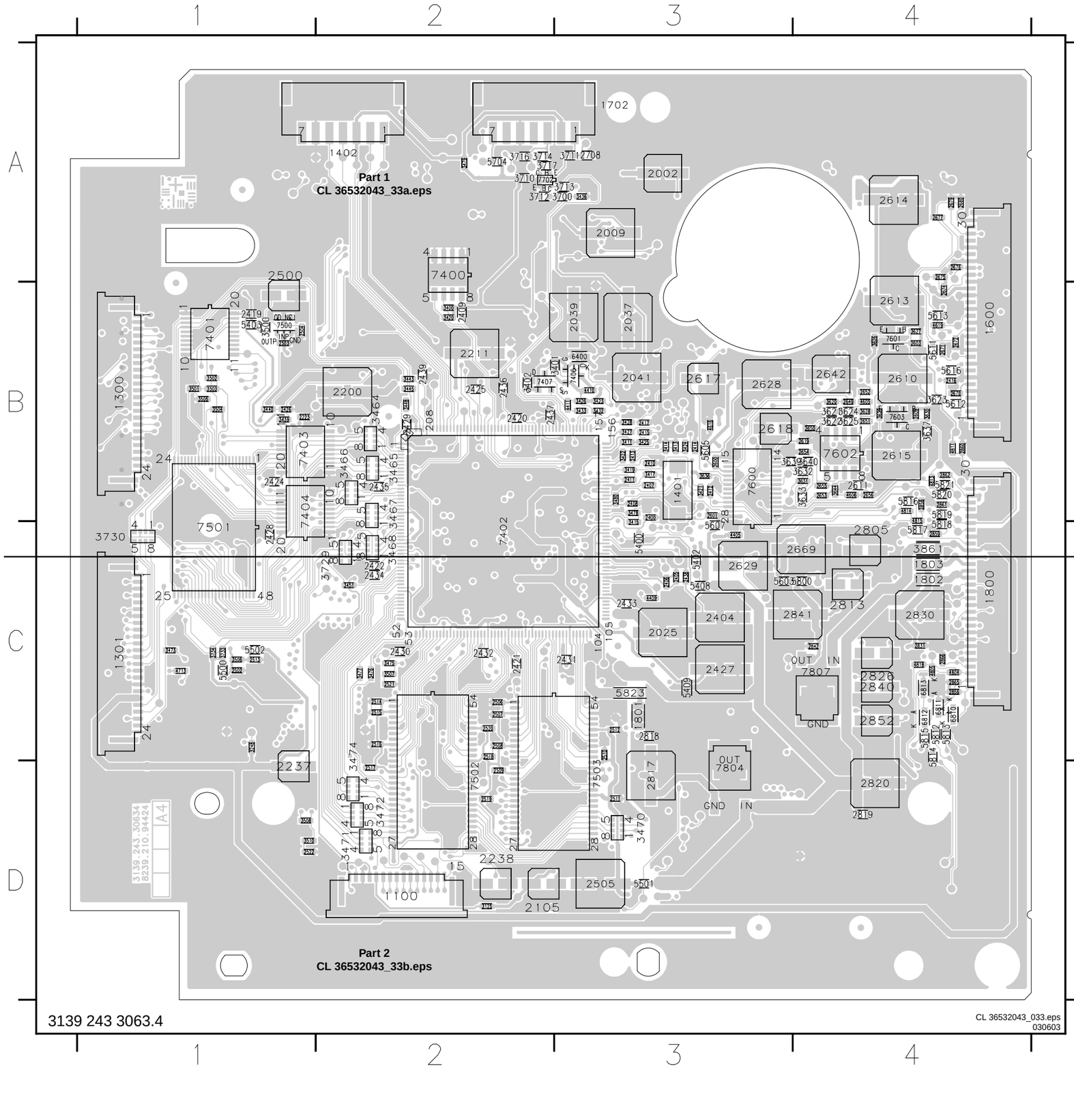


CL 36532043_32a.eps
030603

Layout Bare Board (Part 2 Top Side)

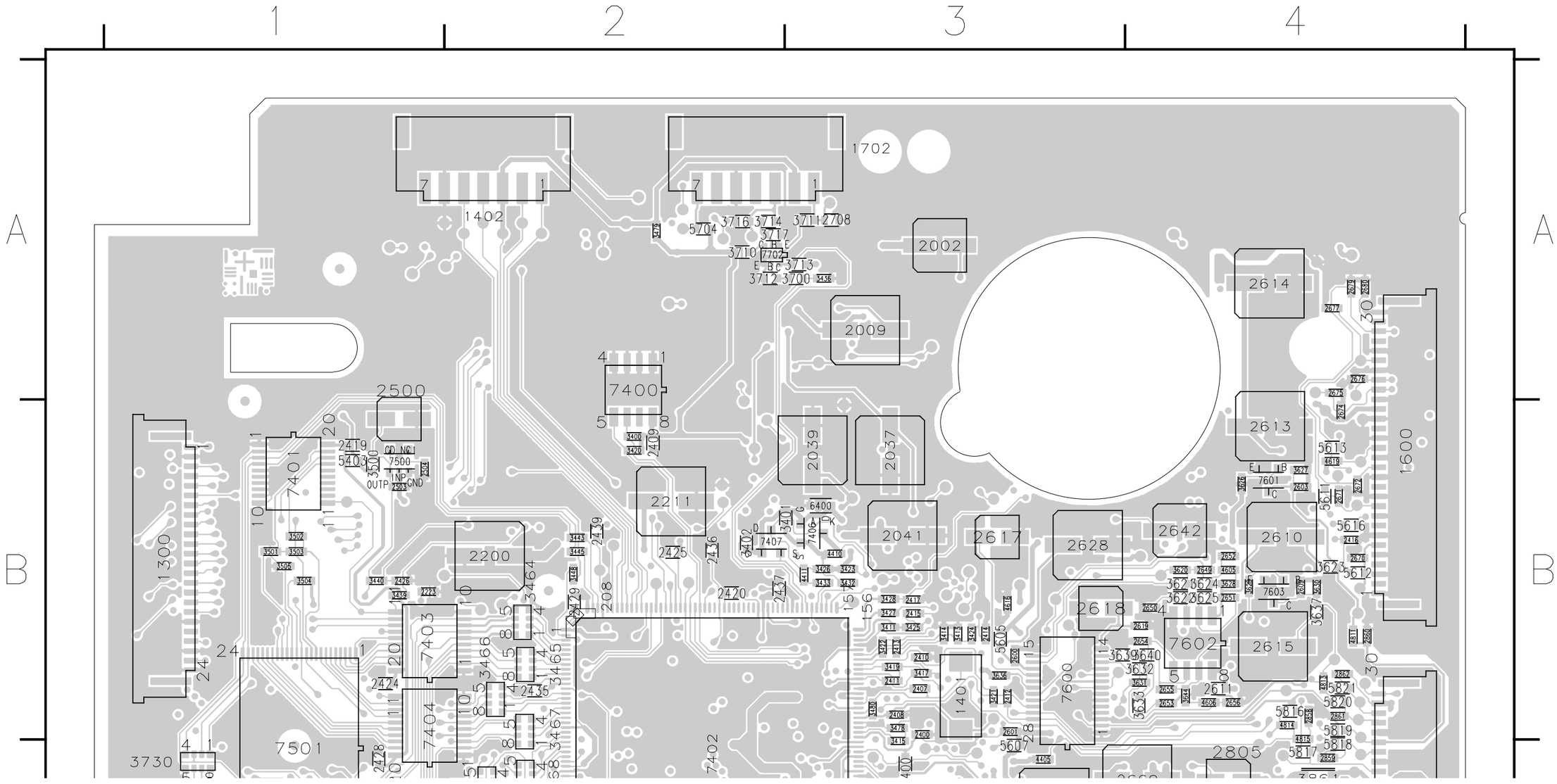


Layout Bare Board (Overview Bottom Side)



1100	D2	2656	B4	3636	B3
1300	B1	2669	C4	3637	B4
1301	C1	2670	B4	3639	B3
1401	B3	2671	B4	3640	B4
1402	A2	2672	B4	3644	B4
1600	B4	2674	B4	3700	A3
1702	A3	2675	A4	3710	A2
1800	C4	2676	A4	3711	A3
1801	C3	2677	A4	3712	A2
1802	C4	2679	A4	3713	A3
1803	C4	2680	A4	3714	A2
2002	A3	2708	A3	3716	A2
2009	A3	2805	C4	3717	A2
2025	C3	2813	C4	3729	C2
2037	B3	2817	D3	3730	C1
2039	B3	2818	C3	3733	C1
2041	B3	2819	D4	3734	C1
2105	D2	2820	D4	3861	C4
2200	B2	2826	C4	4405	C3
2211	B2	2830	C4	4409	C3
2223	B1	2831	C4	4410	B3
2237	D1	2840	C4	4411	B3
2238	D2	2841	C4	4605	B4
2400	B3	2842	C4	4606	B4
2404	C3	2852	C4	4616	B3
2405	C3	2856	C4	4619	B4
2406	C3	2858	B4	4713	C1
2407	B3	2859	C4	4804	C4
2408	B3	2860	B4	4805	C4
2409	B2	2861	B4	4811	B4
2410	B3	2862	B4	4813	B4
2411	B3	2865	C4	4814	B4
2412	B3	2866	C4	4815	B4
2413	B3	3125	D2	4818	C4
2414	B3	3248	C1	5400	C3
2415	B3	3400	B2	5402	C3
2416	B4	3401	B3	5403	B1
2417	B3	3402	B2	5408	C3
2419	B1	3411	B3	5409	C3
2420	B2	3413	B3	5500	C1
2421	C2	3414	B3	5501	D3
2422	C2	3415	C3	5502	C1
2424	B1	3417	B3	5603	C3
2425	B2	3419	B3	5605	B3
2426	B1	3420	B2	5607	C3
2427	C3	3421	B3	5611	B4
2428	C1	3422	B3	5612	B4
2429	B2	3423	B3	5613	B4
2430	C2	3424	B3	5616	B4
2431	C3	3425	B3	5704	A2
2432	C2	3426	B3	5800	C4
2433	C3	3427	B3	5812	C4
2434	C2	3428	B3	5813	C4
2435	B2	3432	B3	5814	C4
2436	B2	3433	B3	5815	C4
2437	B2	3436	A3	5816	B4
2438	C3	3439	B1	5817	C4
2439	B2	3440	B1	5818	C4
2500	A1	3443	B2	5819	B4
2502	C1	3445	B2	5820	B4
2503	B1	3448	B2	5821	B4
2504	B1	3451	C2	5823	C3
2505	D3	3464	B2	6400	B3
2506	C2	3465	B2	6810	C4
2507	C2	3466	B2	6811	C4
2508	C2	3467	B2	6812	C4
2509	D2	3468	C2	6813	C4
2510	C3	3470	D3	7400	A2
2511	D3	3471	D2	7401	B1
2512	C3	3472	D2	7402	C2
2513	C1	3473	C1	7403	B1
2514	C2	3474	C2	7404	B1
2515	C2	3475	C2	7406	B3
2516	C2	3476	C2	7407	B2
2517	D2	3477	C2	7500	B1
2518	C2	3478	B3	7501	C1
2519	D2	3479	A2	7502	D2
2520	C2	3480	B3	7503	D3
2521	C2	3500	B1	7600	B3
2522	D1	3501	B1	7601	B4
2600	B3	3502	B1	7602	B4
2601	B3	3503	B1	7603	B4
2603	B4	3504	B1	7702	A2
2609	B4	3505	B1	7804	D3
2610	B4	3506	C1	7807	C4
2611	B4	3507	C2		
2613	B4	3508	D1		
2614	A4	3510	D1		
2615	B4	3620	B4		
2617	B3	3621	B4		
2618	B3	3622	B4		
2619	B4	3623	B4		
2628	B3	3624	B4		
2629	C3	3625	B4		
2642	B4	3626	B4		
2649	B4	3627	B4		
2650	B4	3628	B4		
2651	B4	3629	B4		
2652	B4	3630	B4		
2653	B4	3631	B4		
2654	B4	3632	B4		
2655	B4	3633	B4		

Layout Bare Board (Part 1 Bottom Side)



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030603

Layout Bare Board (Part 2 Bottom Side)

8. Alignments

Not applicable.

9. Circuit Descriptions, List of Abbreviations, and IC Data Sheets

Index of this chapter:
1. Introduction
2. Loader
3. Mono Board
4. Abbreviations
5. IC Data

Notes:
- For a good understanding of the following circuit descriptions, please also check the diagrams in chapter 6 and 7.

9.1 Introduction

The DVD-SD5.31 is the fifth generation DVD Standard Design Module (ATAPI based) from Philips Video Systems.
The SD5.31 module consists of:
- Tohei TD_S202 Slot-in loader
- ALi M5705/SP3721 front-end processor
- ATAPI bus interconnection between front-end and back-end
- LSI Logic ZiVA-5 back-end DVD decoder / host processor
- Front-end (engine) and back-end software.

9.2 Loader

The Tohei slot-in loader has an optical unit consisting of two lasers, one for CD with a wavelength of 780 nm, and one for DVD with a wavelength of 650 nm. The SP3721A front-end chip (item 7002) controls the data from these lasers, and the supply to them.

When the user slots in a disc, the block diagram below shows, how the disc will be detected and pulled in. The +12VSTDBY source is always present in order to keep the optocoupler circuit functioning. Upon detection of the incoming disc, the Front Panel will be interrupted and a "Power wake-up" signal is send to turn on the Power module to the DVD module. The disc will then be pulled in and reading begins (actual circuit may differ slightly from this).

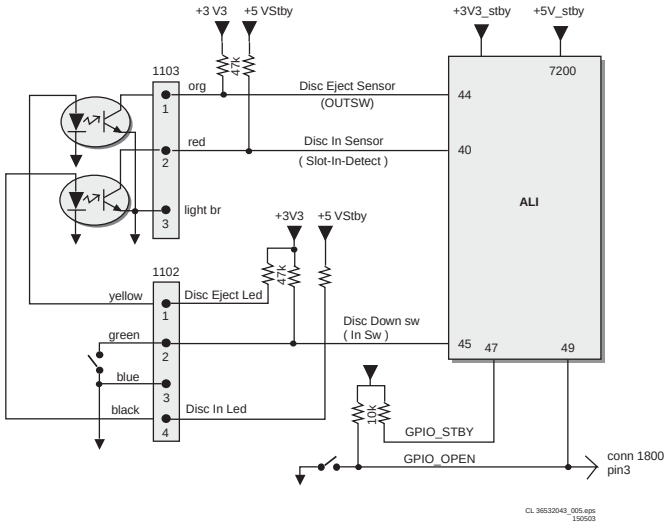


Figure 9-1 Loader sensor

9.3 Mono Board

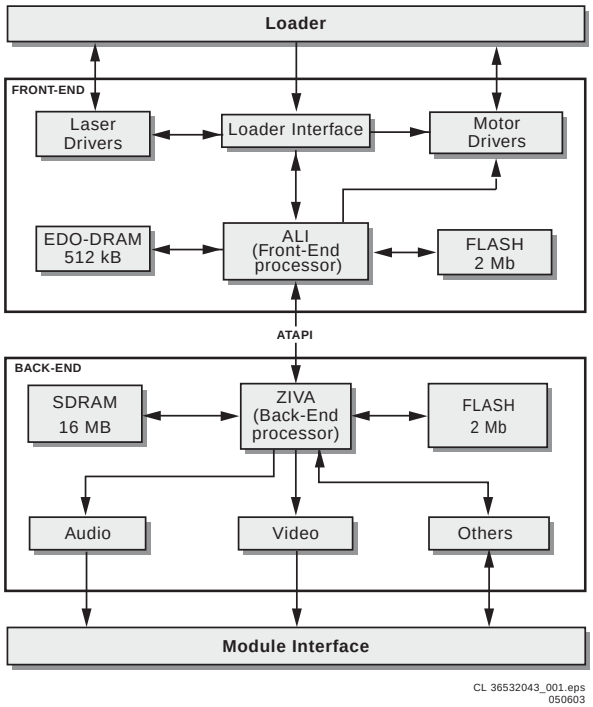


Figure 9-2 SD5.31 Block diagram.

9.3.1 Front-end: the Servo Part

The front-end consists of:
- The Loader Interface.
- DVD Front-End Processor.
- Program Memory.

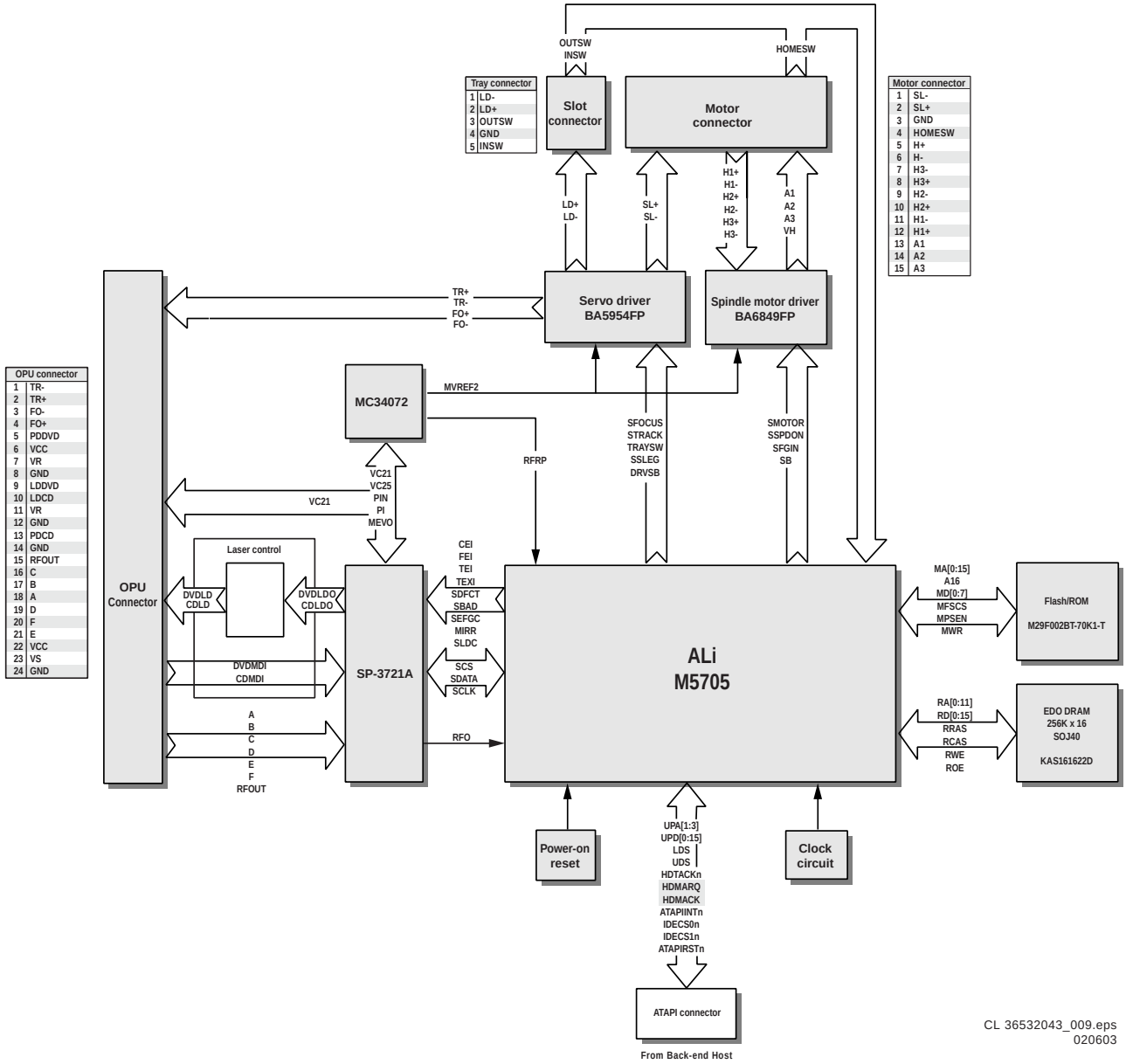


Figure 9-3 Block diagram front-end.

Loader Interface

The SP3721A is a single chip analogue front-end IC that contains the servo functions, RF attenuator, AGC and programmable equalizer/filter for the CD/DVD drive system and a dual auto laser power control (APC) circuit to support the twin laser system.
The servo block includes mirror detection, defect detection, dual auto laser power control, tracking zero crossing, focus error, centre error and tracking error detection circuits.

RF Interface

The SP3721A provides the RF interface for both DVD and CD signals. DVD signals can be AC coupled into the device through the differential input pins DVDRFP and DVDRFN, while the CD signal interface is single-ended through the CDRF pin. Both inputs are coupled to the PUHRF line from the OPU.

Servo Interface

The SP3721A also provides the voltage-input interface for photo detector signals used in the servo block, to detect centre errors, focusing errors, and tracking errors. These signals include the output from the quad cell photo detectors (A, B, C, D) and CD photo detectors (E, F, PD1, PD2), which are directly connected from the pick-up.
The servo block includes focusing error detection, tracking error detection, centre error detection, defect detection, tracking zero crossing output, mirror detection and dual auto laser power control circuits.
The servo interface accommodates both single laser and twin-laser pickups.

Auto Laser Power Control (APC)

The SP3721A provides dual APC circuits for a DVD laser and a CD laser. The DVD APC circuit has a selectable high or low power mode of operation. The CD APC circuit is fixed at low power or high gain mode.
Only one APC circuit can be operating at any given time. When either or both of the APC circuits are "off", the output will be fixed to the supply voltage.
Transistors 7000 and 7001 will function as laser drivers and are controlled via the DVDLDO and CDLDO laser power control lines.

DVD Front-End Processor

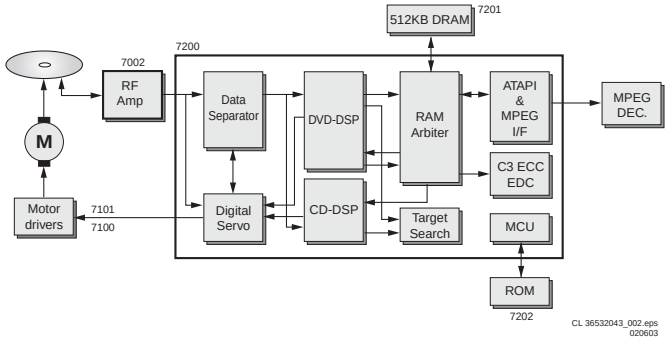


Figure 9-4 Block diagram.

The ALI M5705 includes:
- An embedded micro controller.
- A DVD-decoder.
- A CD/CD-ROM decoder.
- A RAM buffer interface.
- An ATAPI interface.
- A data channel.
- A digital servo controller.

The M5705 can support up to 32-speed CD-ROM and 6-speed DVD-ROM systems. It can playback not only the standard format of DVD-ROM and DVD-R disk, but also all the various CD-ROM disk types such as CD-DA, VCD, CDI, Photo CD, Karaoke CD, CD-plus, Enhanced CD, CD-R, etc.
Together with the SP3721A RF signal processor, an audio DAC, a RAM buffer, and motor drivers, the M5705 is configured as a CD/DVD-ROM system. It also integrates MPEG-2 interface (or so-called local bus) and has an ATAPI based interface bus.

The M5705's digital servo implements the focus, tracking, sledge and spindle servo loop. It also provides an auto-adjustment method for adjustment-free CD/DVD systems. It also provides a stable layer jump solution for reading data from dual layer DVD discs. This feature makes the playback go smoothly at the point of layer change.

The M5705 includes an embedded micro controller, which is compatible with Intel 8032. It also supports an automatic system firmware download function for upgrading the system firmware directly from ATA interface or CD-R discs recorded with new version firmware.

The ATA interface can transfers data in Programmed I/O (PIO) mode. The local bus signals for directly connecting to an MPEG decoder share the pins with ATA interface.

Features M5705
- Data Separator
  - Built-in data slicer and data PLL for data recovery from RF signal.
  - Supports digital/analogue slice level adjustment.
  - Built-in auto calibration function.
  - Built-in auto wire range control function.
- DVD-DSP
  - Built-in synchronous pattern/ID detection /protection/ separation.
  - Built-in EFM+ (8 to 16) demodulation circuit.
  - n Built-in high performance RSPC ECC circuit.
  - Supports up to 6X DVD-ROM system with ECC correcting "on the fly".
  - Built-in descrambler/EDC circuit.
- CD-DSP
  - Synchronous pattern detection, protection, and interpolation.
  - Built-in EFM demodulation circuit, subcode demodulation circuit.
- Digital Servo
  - Built-in A/D and D/A converters for servo control signals processing.
  - Built-in digital controller for focus, tracking servo control of CD/DVD systems.
  - Built-in CLV/CAV auxiliary function for spindle servo control.
  - Built-in "Seek Sensor" auxiliary circuit for seek control.
  - Automatic adjustment of focus servo and tracking servo, for loop gain, offset and balance.
  - Built-in RF-gain automatic adjustment function.
  - Built-in AFC circuit and APC circuit for CLV and AFC circuit for CAV spindle servo of CD/DVD systems.
  - Built-in defect and shock protection function.
- DRAM Interface
  - Supports up to 16 Mb EDO DRAM and SDRAM.
  - Separate buffer address pointers and automatic address calculation that save firmware effort.
  - Read-ahead cache scheme for multimedia isochronous transfer.
  - Protection logic preventing uncorrected sectors being released to the host.

Memory
A 512 KB EDO-DRAM (item 7201) is used as a data buffer and error correction for ATAPI.

A 2 Mb flash memory (item 7202) is used to store the front-end software, used by the ALI M5705 front-end controller. Since actual addressable space is 1 Mb, the MSB address pin of this memory is jumpered to "low".

9.3.2 Interface

The interface between front-end and back-end is done via an ATAPI interface.
First, a little about the acronyms. IDE and ATA are synonymous. ATA is short for AT-attachment, referring to the original IBM AT computer. IDE stands for Integrated Drive Electronics. The ATA acronym is preferred today over IDE. Why is it called AT-attached? The signals on the 40-pin ATA ribbon cable follow the timings and constraints of the ISA system bus on the IBM PC AT. ATAPI stands for AT Attachment Packet Interface (ATAPI).
Hosts control ATAPI devices are using SCSI (Small Computer System Interface) command packets. The SCSI command packets are transported over the ATA interface, instead of the parallel SCSI bus (ATA/ATAPI-6).
Different devices accept different sets of SCSI command packets. There are some differences in command packet format between ATAPI and SCSI. Mostly, these are simplifications, i.e. features are missing in ATAPI that would appear on a SCSI device. There are some areas, though, where ATAPI defined new commands and responses.

IDE and ATA are, as mentioned earlier, one and the same thing: a disk drive implementation designed to integrate the controller onto the drive itself, thereby reducing interface costs, and making firmware implementations easier.
One of the disadvantages of ATA is that it was designed for hard disks only. That was fine back when a high end PC shipped with just a floppy drive and a 40 MB hard disk, but today CD-ROM and tape drives are commonplace devices that should preferably run off a single low-cost interface. The ATA Packet Interface (ATAPI) is a standard designed for devices such as CD-ROMs and tape drives that plug into an ordinary ATA (IDE) port.

9.3.3 Back-end: the Digital Part

The back-end consists of:
- DVD back-end processor
- External memory
- Audio output
- Video output

- Miscellaneous

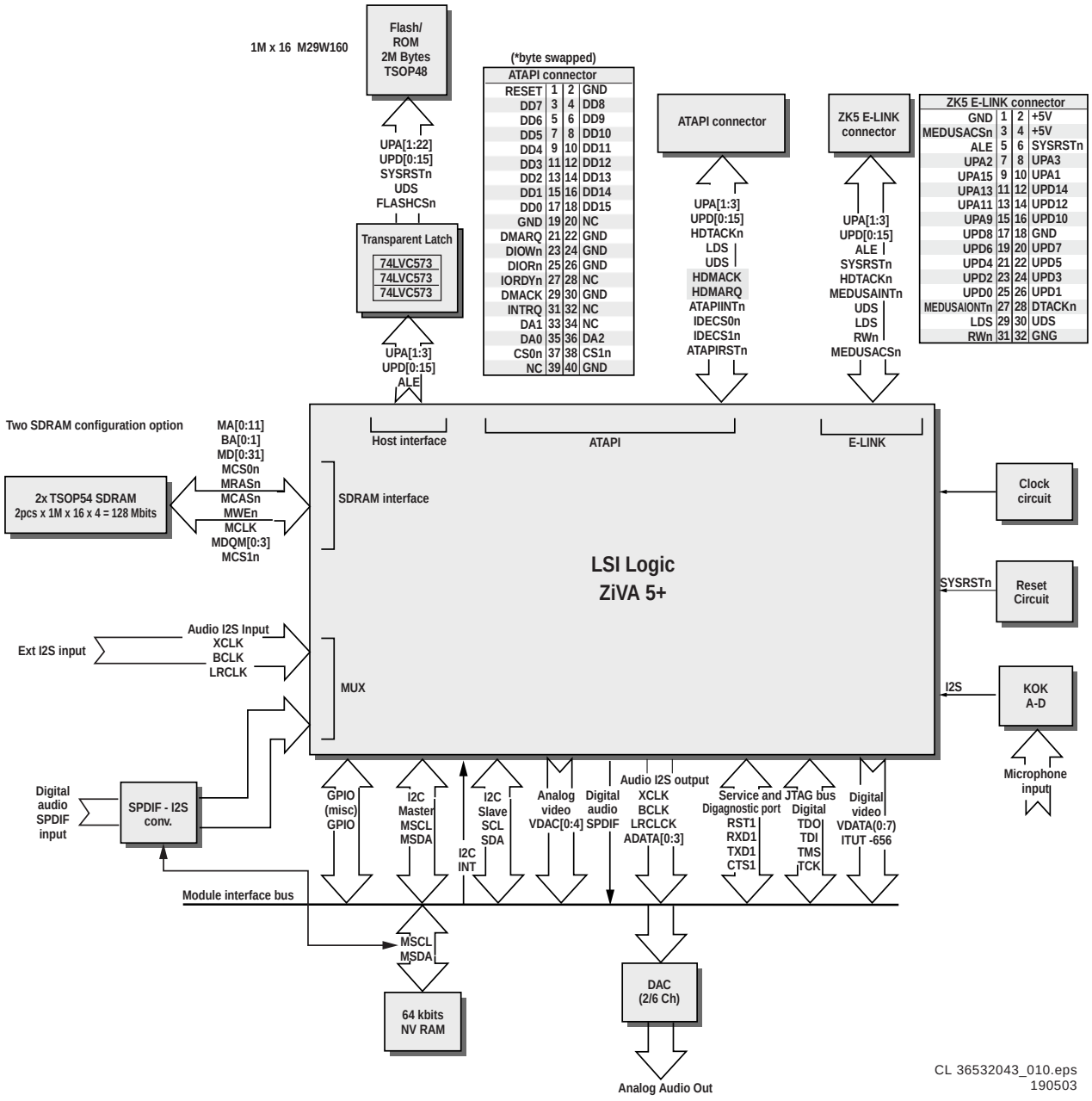


Figure 9-5 Block diagram back-end

DVD Back-end Host Processor

The SD5.31 is designed for the LSI-Logic ZiVA-5 family.

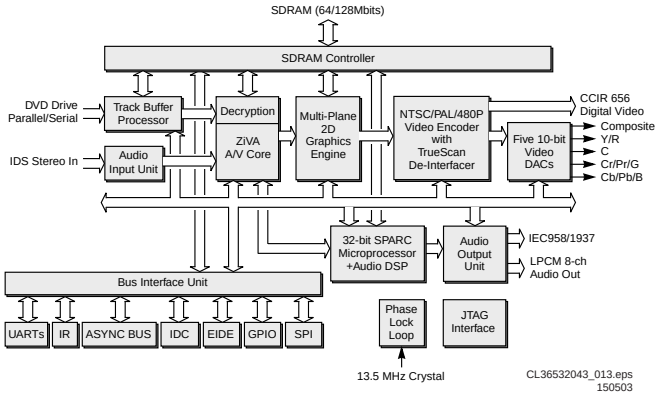


Figure 9-6 ZiVA-5 Block Diagram

Some of the DVD related features of this IC are:

- Video decoder supports MPEG1 and MPEG2
- Audio decoder supports AC-3, MPEG1, MPEG2, DTS, PCM, S/PDIF, and MP3.
- PAL/NTSC video encoder with simultaneously Y/C, CVBS and RGB/YUV outputs
- The video encoder supports Closed Caption and allows MacroVision 7.0/6.1
- Full screen On Screen Display (OSD) generator
- On-chip PLLs to generate all necessary clocks (as reference a 13.5 MHz xtal is used).

CPU

The ZiVA-5 incorporates a 32-bit SPARC host CPU for audio processing and special features. The SPARC CPU is designed to act as the system host processor (thus removing the requirement for an external host CPU with associated memory).

Track Buffer Processor
An integrated Track Buffer Processor parses, frames, and performs error processing on all DVD and CD sector types.

Flexible DVD Drive Interface
The DVD drive input of ZiVA-5 supports most serial stream and parallel stream type drives, as well as EIDE (ATAPI) drives.

Video Encoder
It incorporates a video encoder with five video DACs to provide high-quality video. The video encoder supports PAL, NTSC, RGB, SCART, interlaced 480i, and progressive 480p YPbPr components, and is fully programmable for colour saturation, contrast, brightness, and sharpness.
The video encoder is compliant with both MacroVision 7.1.L.1 for interlaced video (PAL, NTSC) and MacroVision AGC 1.03 for Progressive scan (480p). In addition to CSS, ZiVA-5 provides Copy Protection for Pre-recorded Media (CPPM), Copy Protection for Recorded Media (CPRM), and audio watermark detection, all of which are required for DVD-Audio. It is fully compatible with DVD-Video, DVD-Audio, Chaoji-VCD (CVD), SuperVCD, VCD, CD-DA, and CD-ROM formats such as MP3.

On-chip Peripherals
On-chip peripherals include Inter-Device Communications (IDC) master/slave interface, two standard UARTs, SPI, and a direct multimode infrared (IR) input. All peripheral interfaces can be configured as GPIO pins for added flexibility.

Input
Input data comes via the ATAPI-bus. The front-end interface of the ZiVA-5 accepts DVD, CD, and CD-DA information.

Signal Processing
For video, the input data stream is decoded to the appropriate MPEG, Sub Picture, and OSD data streams, after which they are fed to the PAL/NTSC encoder. This cell will convert the digital MPEG/Sub Picture/OSD stream into a standard base band signal and into RGB components. It handles interlaced and non-interlaced data, can perform CC/TXT encoding, and allows MacroVision copy protection.

For audio, the processing cell is a fully compatible DTS, Dolby Digital (AC-3), MPEG1, MPEG2, PCM decoder, capable of decoding 5.1 and 2 channel streams.

Memory
The 2 MB flash memory (item 7501) is used to store the application software. During normal operation, the application is executed live from the (2 x 16 bit = 32 bit) SDRAM.
A 64 kb NVRAM (item 7400) is used to store the factory/user settings. This memory is connected to the master I2C bus.

Audio Output
The audio interfaces available are I2S and S/PDIF for digital audio output, and (optional) I2S karaoke microphone input.

I2S audio
The ZiVa-5 is capable of 2/6-channel PCM output. These channels can be configured to output 5.1 Dolby Digital, DTS, etc.
- DA_DATA0 (pin 150): Down mixed left and right (LtRt).
- DA_DATA1 (pin 151): Front left and right (LoRo).
- DA_DATA2 (pin 154): Surround left and right (LsRs).
- DA_DATA3 (pin 155): Centre and subwoofer (CSw)

S/PDIF
The S/PDIF signal level (item 7402, pin 156, IEC_958) is 1Vp-p at module interface. To meet the complete S/PDIF specifications, an external de-coupling circuit (item 7810, diagram M8) is implemented.

Audio Mute
This is a global audio mute, which blocks the final analogue stage, and affects all channels simultaneously. The main objective of this signal is to prevent switching noise at the audio output as the player changes its mode of operation.

Apart from this global mute, additional audio (digital) mute is applied to all stages of the audio path where possible. For example, the decoder should apply digital mute to the audio stream as and when needed. Note that the global mute does not provide adequate attenuation to normal audio signals and should not be used as an alternative to digital mute.
The MUTE pin must be set "high" immediately upon power-up to avoid audible "plops". We can distinguish three states:
- **During normal operation.** When the MUTE line is activated (high), transistor 7600 will switch "on", biasing 7607, 7609, 7601, and 7603 to turn "on".
- **During initial power-up from standby.** No mute signal available, +5VSTBY will bias transistors 7607 and 7609 to turn "on", which in turn switch "on" transistors 7601 and 7603.
- **During power off.** No standby voltage available, the +5 V across C1 and C2 will bias 7608 and 7615 to switch "on".

Video Output

Analogue video
The digital output of the PAL/NTSC decoder is converted to the analogue domain by on-chip DACs. The ZiVA-5 is capable of 5-channel analogue video. Three channels are in RGB/YUV format (pins 125, 122, and 120), while the other two channels are C and CVBS (pins 128 and 131). Table below shows the multiplexed nature of the ZiVA-5 internal video DACs and the jumper options on the PWB to cater for the different output configurations:

Table 9-1 Video DAC overview

Mode	Name	DAC1	DAC2	DAC3	DAC4	DAC5
1	SCART RGB	CVBS	CVBS	G	B	R
2	SCART Y/C	CVBS	Y	C		
3	SCART Y/C + RGB	Y	C	G	B	R
4	Non-com-ponent	CVBS	C	Y		
5	Component	CVBS	C	Y	Pb (U)	Pr (V)
6	480p			Y	Pb (U)	Pr (V)

Via jumpers 4807, 4806, and 4816 selection is made for the required video output on connector 1800. DACs that are not in use are turned "off".

A video output buffer (see diagram M8) is implemented: a filter stage (e.g. circuit around items 5801/ 5802 for CVBS) and a drive stage (e.g. item 7800 for CVBS).

Miscellaneous I/O signals

Chip Selects

Table 9-2 Chip select overview

CS nr.	Device	Ziva-5 Pin nr.
0	Flash memory	195
2	E-Link daughter card	193
3	IDE0	192
4	IDE1	191

Interrupts

Table 9-3 Interrupt overview

HIRQ nr.	Device	Ziva-5 Pin nr.
0	E-Link daughter card	24
1	ATAPI	184
2	N/u	116

SCART
Previously, an on-board circuit switches the 0_6_12V signal to be 0V, 6V or 12V. This circuit is removed. Instead, the SCART0 and SCART1 signals are now directly available at the module interface (pins 3 and 4 of connector 1800).

Miscellaneous

I2C
The SD5.31 module has two I2C buses. The slave I2C is using hardware I2C (because of its speed) and the master uses software I2C via GPIO ports.
The master I2C bus controls all on-board devices e.g. NVRAM, audio DAC etc., while the slave I2C bus is used to connect to an external processor e.g. a TV or Audio set microprocessor, which acts as the I2C master controller.
An additional signal (I2C_INT) can be used to flag to the external processor when data is available in the slave mode.

I2S
Two external I2S inputs can be connected to Ziva-5. However, only one input can be used at any one time as they are multiplexed inside the chip. On SD5.31, one input is coming from an SPDIF-I2S converter (e.g. external source on an audio set), while the other is from an external source (e.g. a TV receiver audio section). The slash version of the module will decide which input is used. Only 2-channel PCM I2S up to 96 kHz is currently supported.

Service Port Buffer

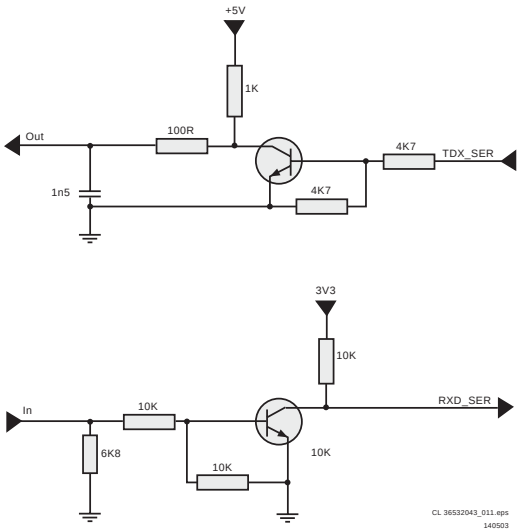


Figure 9-7 Service Port Buffer

The service port (see diagram M7) is simplified to reduce cost. The unused RTS and CTS lines are no longer connected. A transistor buffer (item 7702) is used instead of the Schmitt Trigger buffer.

9.3.4 Motor drivers

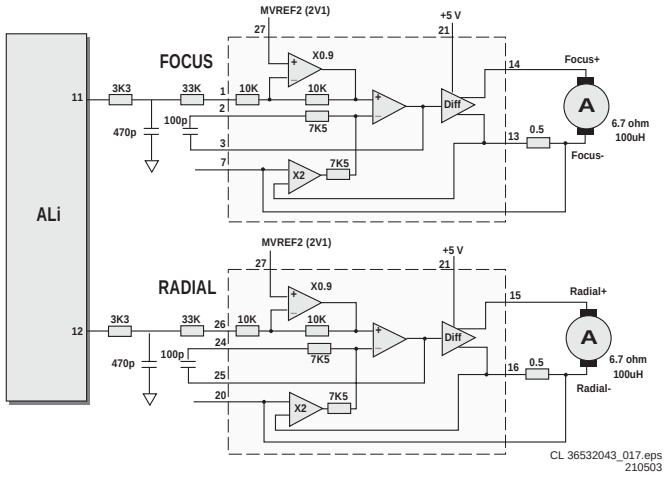


Figure 9-8 Block diagram motor drivers

The following motor driver ICs are controlled by the Ali M5705:
- The spindle motor driver.
- The servo motor driver.

Both ICs require a reference voltage (MVREF2) of 2.1 V. This voltage is generated with IC 7002 (pin 26 provides a reference bias voltage of 2.5 V) and buffered with OpAmp 7003-A.

Spindle Motor Driver
The spindle motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the (hall) motor unit. They drive the motor IC (BA6849FP, item 7101).

BA6849FP Features:
– Three-phase, full wave, pseudo-linear drive system.
– Built-in power save and thermal shutdown functions.
– Built-in current limiter and Hall bias circuits.
– Built-in rotation direction detector.
– Built-in reverse rotation prevention circuits.

Servo Motor Driver
The BA5954FP (item 7100) is a 4-channel motor driver with built-in current feedback. Sensing is done via resistors 3110// 3112 for focus signals (pin 7) and resistors 3114//3115 for the tracking signals (pin 20).
This driver controls the following motors:
- Sledge motor (SL+ and SL-).
- Loader motor (LD+ and LD-).
- Focus motor (FO+ and FO-).
- Tracking motor (TR+ and TR-).

BA5954FP Features:
– Wide dynamic range.
– Level shift circuit built-in.
– Thermal shutdown circuit built in (at 175 deg. C.).
– Stand-by mode built-in.

9.3.5 Power Supply (diagram M7)

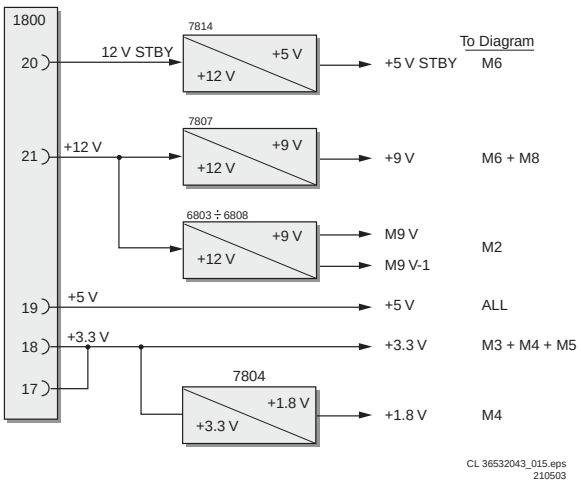


Figure 9-9 Power Supply Block Diagram

The main power supplies to the module are 3.3 V, 5 V, 12 V, and 12VSTBY (input via connector 1800).
On-board linear regulators are used to generate the 1.8 V (required by the ZiVa-5), the +9 V (required by the motor drivers), and the +5VSTBY (required by the audio muting circuitry).
The front-end section mainly uses the 5 V and 9 V, while the back-end section mainly uses the 3.3 V and 5 V.
See table for the normal operating conditions.

Table 9-4 Normal operating conditions

Voltage name	Input voltage (VDC / V)				Ripple noise voltage(VPP / mV)	Current consumption (IDC / mA)			
	Power-on			Power-off		Power-on			Stby
	Min.	Typ.	Max.			Min.	Typ.	Max.	
+3.3V	3.135	3.30	3.465	< 0.10	50		1.2 A	1.3 A	0
+5V	4.75	5.00	5.25	< 0.10	50		400 mA	700 mA	0
+12V	10.80	12.00	13.20	< 0.10	200		300 mA	780 mA	0
+12VStby	10.80	12.00	13.20	< 0.10	200		60 mA	65 mA	65 mA

Power sequence timing

The module operates in "power-on", "power-off", and "standby" modes. In the standby mode, only the disc-in detection circuit is powered by the +5VSTBY (derived from +12VSTBY via regulator 7814). When the user slots in a disc, it will be automatically detected and the Front Panel controls (from the DVD-player or TV-set) will be interrupted via the FRONT_IRQ line from the ZiVA-pin 159. A Power wake-up signal is then sent to turn on the Power module in order to apply power to the DVD module. The disc will be pulled in, and reading begins.

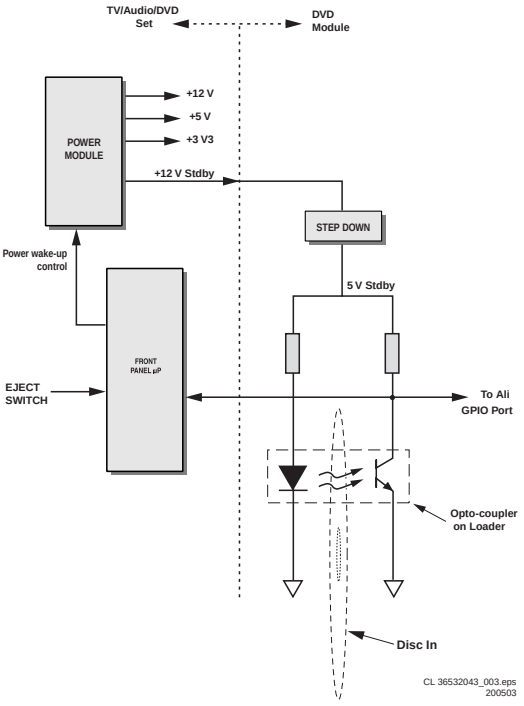


Figure 9-10 Slot-in Auto Detect

Reset Circuit

Reset of the module is done via a separate "master reset" circuit, which senses the +5V. The output is pulled to +3V3.

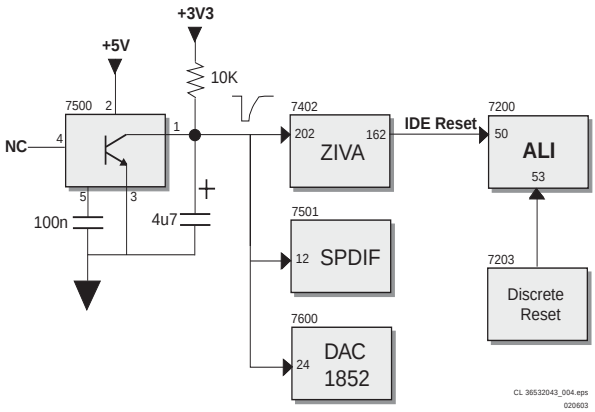


Figure 9-11 Reset circuit

To ensure proper power recycling of the module, the following timing should be observed:

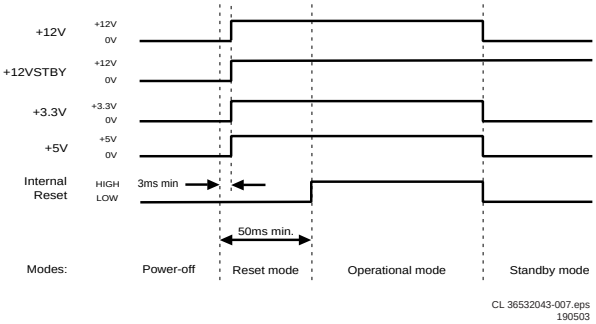
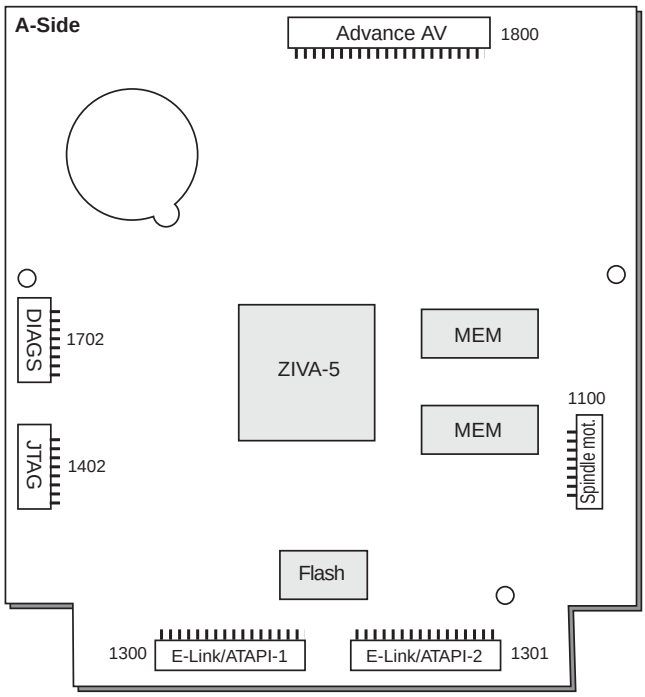


Figure 9-12 Power supply timing

9.3.6 PWB overview

The board interfaces are located on both sides of the board, as shown below:



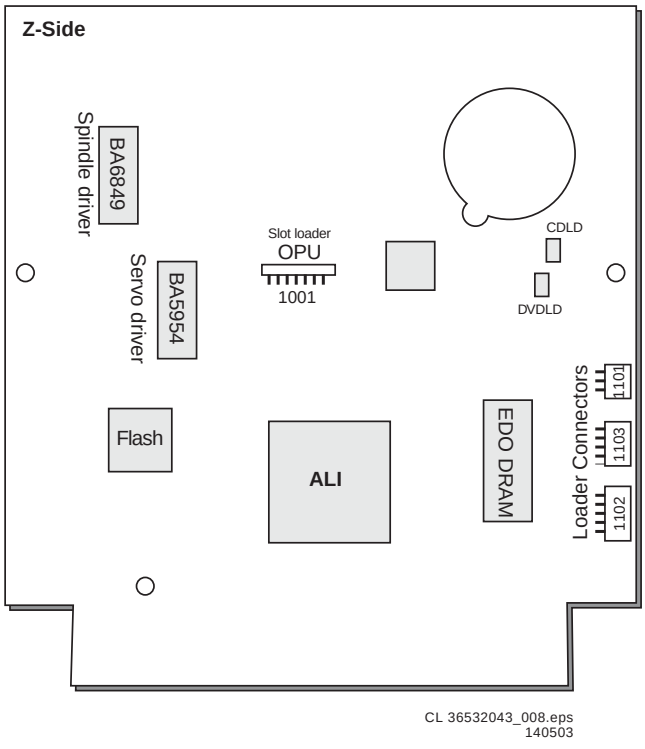


Figure 9-13 Board connections

9.4 Abbreviation list

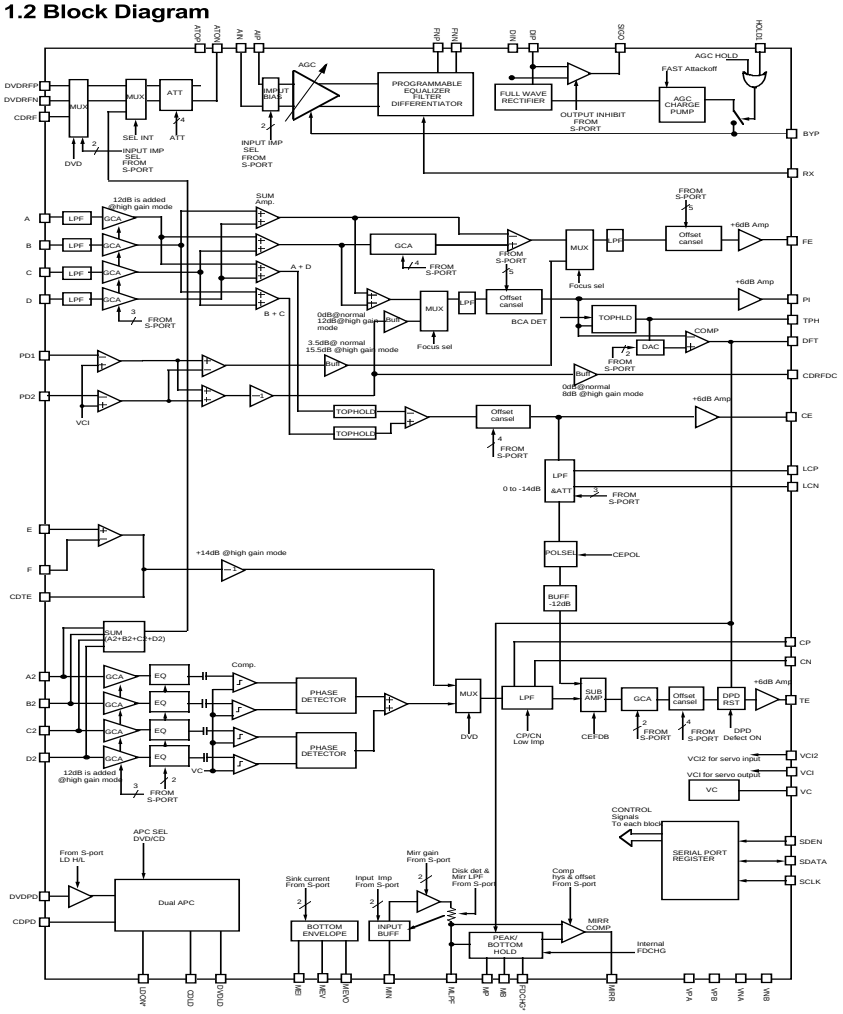
AC3	Older term for Dolby Digital
ADC	Analogue to Digital Converter
ASD	Architecture Standard Design
ATAPI	AT Attachment Packet Interface
AM	Amplitude Modulation
AV	Audio Video
BE	Basic Engine
BST	Boundary Scan Testing, IC testing method
ComPair	Computer aided rePair
CD	Compact Disc
CD-DA	CD Digital Audio
CD-ROM	CD Read Only Memory
CVBS	Composite Video Blanking and Sync
CS	Chip Select
DAC	Digital to Analogue Converter
DAIO	Digital Audio Input Output
DENC	Digital Encoder
DFU	Direction For Use: description for the end user
DNR	Dynamic Noise Reduction
DRAM	Dynamic RAM
DSD	Direct Stream Digital
DSP	Digital Signal Processing
DTS	Digital Theatre Sound
DVD	Digital Versatile Disc
DVD back-end	DVD digital (MPEG, etc.) decoder part
DVD front-end	DVD servo part (previously called Basic Engine)
EEPROM	Electrically Erasable and Programmable Read Only Memory
EIDE	Enhanced IDE
EFM	Eight to Fourteen bit Modulation
EMC	Electro Magnetic Compatibility
EMI	External Memory Interface (STi55xx)
FFC	Flat Foil Cable
FLASH	Flash memory
HPF	High Pass Filter
HW	Hardware
I2C	Integrated IC bus (signals at 5V level)
I2S	Integrated IC Sound bus (signals at 3.3V level)
IC	Integrated Circuit
IDE	Integrated Drive Electronics
IF	Intermediate Frequency
IO	Input Output
IRQ	Interrupt Request
JTAG	Joint Test Action Group, a 5-pin interface as outlined in standard IEEE 1149.1 providing boundary scan testing (BST)
kbit (kb)	2^10 bit
kByte (kB)	2^20 Byte (1 Byte = 8 bit)
KOK	Karaoke
LFE	Low Frequency Effect (sub-woofer)
LLD	Loss Less Decoder
LPCM	Linear Pulse Code Modulation
LRCLK	Left/Right clock
LSB	Least Significant Bit
LVTTL	Low Voltage Transistor Transistor Logic (3.3V logic)
MACE	Mini All Compact Disc Engine
Mbit (Mb)	2^20 bit
MByte (MB)	2^20 Byte (1 Byte = 8 bit)
MLP	Meridian Lossless Peaking
MPEG	Motion Pictures Experts Group
MPEG1	MPEG standard used by VCD
MPEG2	MPEG standard used by DVD
MP3	Informal audio codex
MSB	Most Significant Bit
NC	Not Connected
NVM	Non Volatile Memory: IC containing TV related data e.g. alignments
OC	Open Circuit
OPU	Optical Pick-up Unit
OSD	On Screen Display
PCB	Printed Circuit Board (see PWB)
PCM	Pulse Code Modulation
PCM_CLK	Audio system clock for DAC
PCM_OUTx	Audio serial output data
PS(U)	Power Supply (Unit)
PWB	Printed Wiring Board (see PCB)
RAM	Random Access Memory
RGB	Red, Green, and Blue colour space
ROM	Read Only Memory
S2B	Serial to Basic Engine, communication bus between host- and servo processor
SCL	Serial Clock I2C
SCLK	Audio serial bit clock
SCSI	Small Computer System Interface
SDA	Serial Data I2C
SDRAM	Synchronous DRAM
S/PDIF	Sony Philips Digital InterFace
SRAM	Static RAM
STBY	Standby
SVCD	Super Video CD
SW	Software
THD	Total Harmonic Distortion
TTL	Transistor Transistor Logic (5V logic)
UART	Universal Asynchronous Receiver Transmitter
uP	Microprocessor
VCD	Video CD
Y/C	Luminance (Y) and Chrominance (C) signal
YUV	Luma and chroma video component (= YCbCr)

9.5 IC Data Sheets

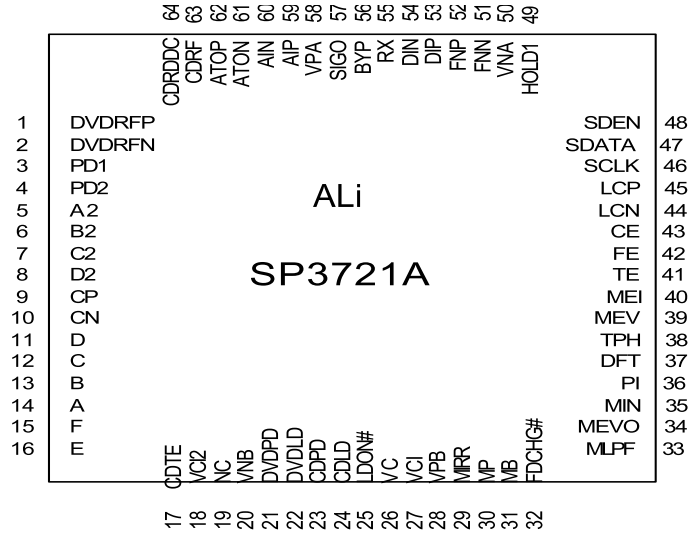
This section shows the internal block diagrams and pin layouts of ICs that are drawn as "black boxes" in the electrical diagrams (with the exception of "memory" and "logic" ICs).

9.5.1 SP3721 (IC7002)

1.2 Block Diagram



2.1 Pin Diagram



CL 36532043_019.eps
050603

Figure 9-14 Internal Block Diagram and Pin Layout

9.5.2 BA6849FP (IC7101)

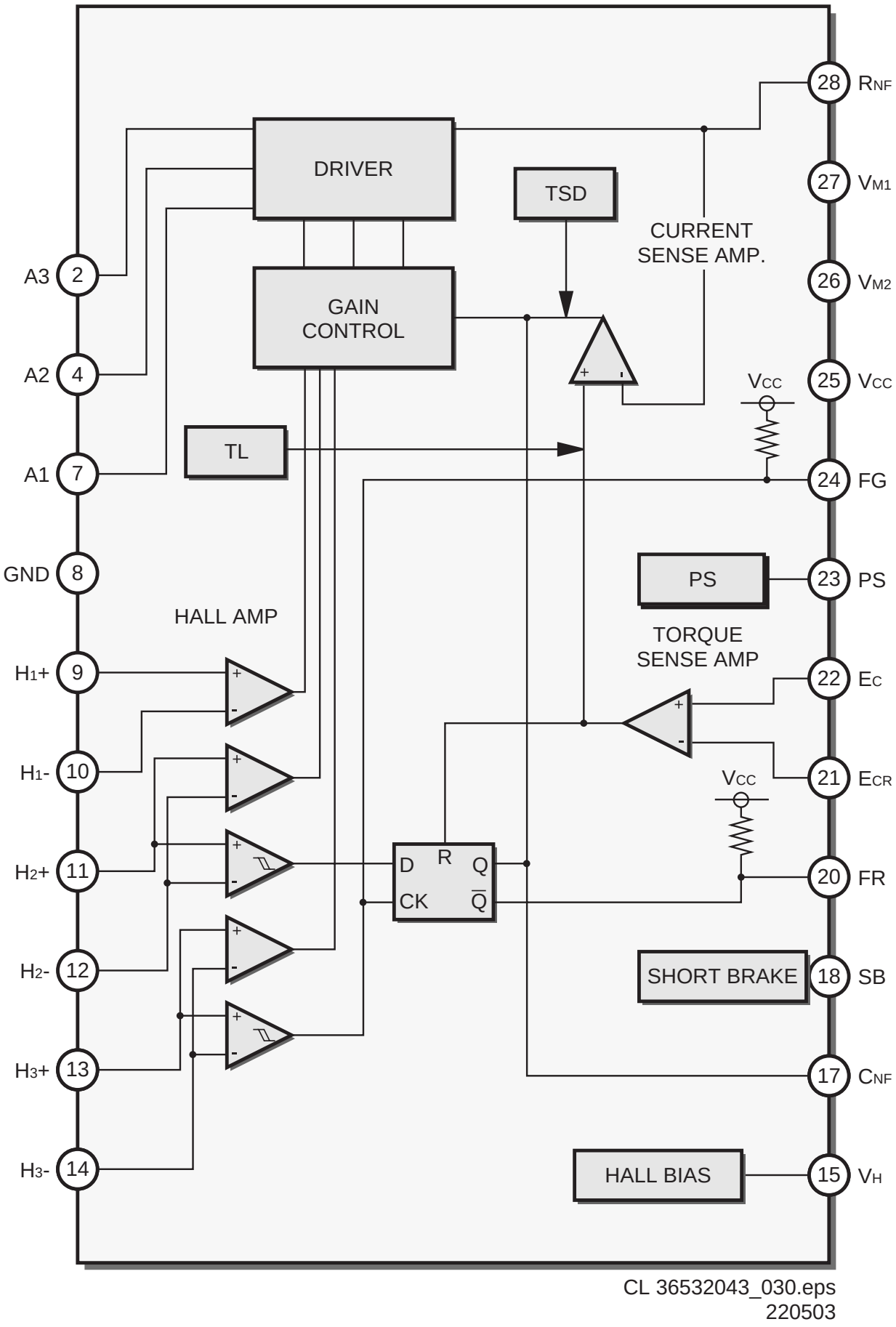


Figure 9-15 Internal Block Diagram and Pin Layout

9.5.3 BA5954FP (IC7100)

BLOCK DIAGRAM

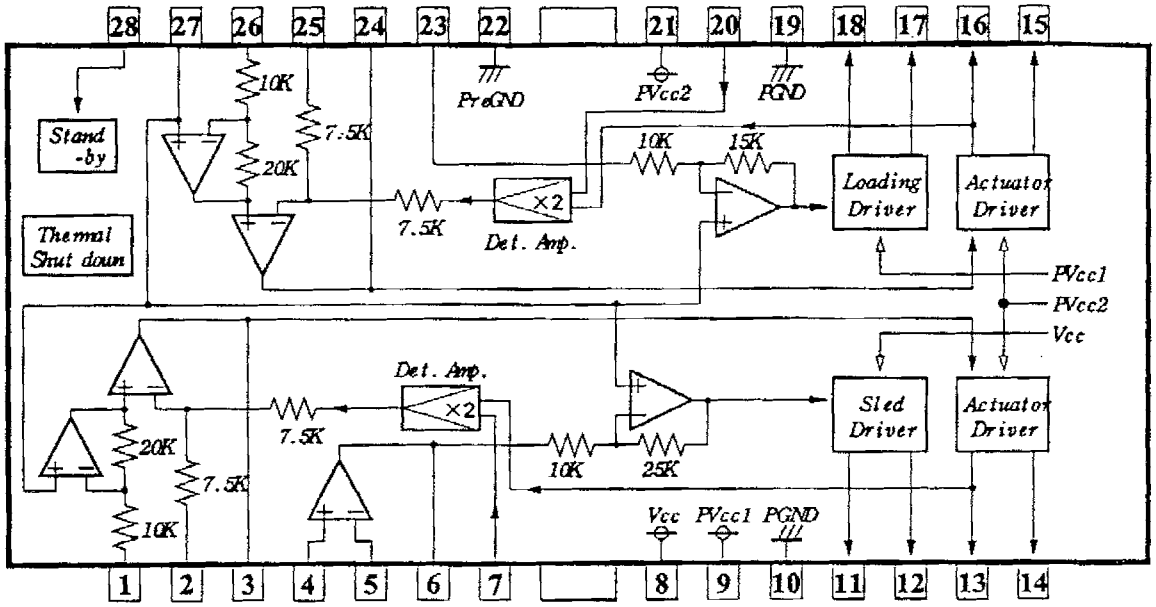


Figure 3

Pin description

No	Symbol	Function	No	Symbol	Function
1	VINFC	Input for focus driver	15	VOTK+	Non inverted output of tracking
2	CFCerr1	Connection with capacitor	16	VOTK−	Inverted output of tracking
3	CFCerr2	for error amplifier	17	VOLD+	Non inverted output of loading
4	VINSL+	Non inverting Input for OP−amp	18	VOLD−	Inverted output of loading
5	VINSL−	Inverting input for OP−amp	19	PGND	GND for power block
6	VOSL	Output of OP−amp	20	VNFTK	Feedback for tracking driver
7	VNFFC	Feedback for focus driver	21	PVcc2	Vcc for power block of actuator
8	Vcc	Vcc for pre−drive block and power block of sled	22	PreGND	GND for pre−drive block
9	PVcc1	Vcc for power block of loading	23	VINLD	Input for loading driver
10	PGND	GND for power block	24	CTKerr2	Connection with capacitor
11	VOSL−	Inverted output of sled	25	CTKerr1	for error amplifier
12	VOSL+	Non inverted output of sled	26	VINTK	Input for tracking driver
13	VOFC−	Inverted output of focus	27	BIAS	Input for reference voltage
14	VOFC+	Non inverted output of focus	28	STBY	Input for stand-by control

notes) Symbol of + and − (output of drivers) means polarity to input pin.
(For example if voltage of pin1 is high,pin14 is high.)

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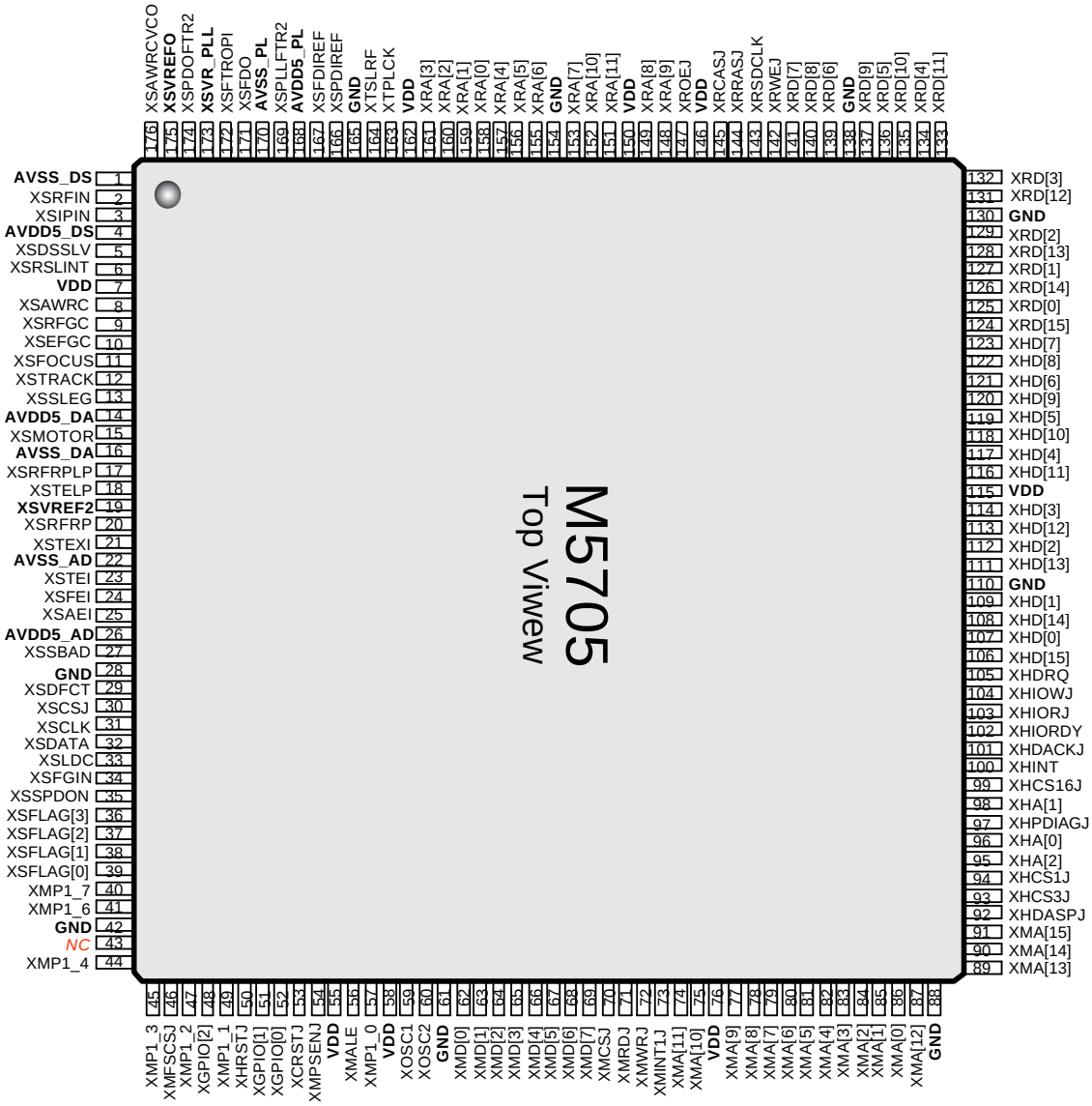
030603

Figure 9-16 Internal Block Diagram and Pin Layout

9.5.4 M5705 (IC7200)



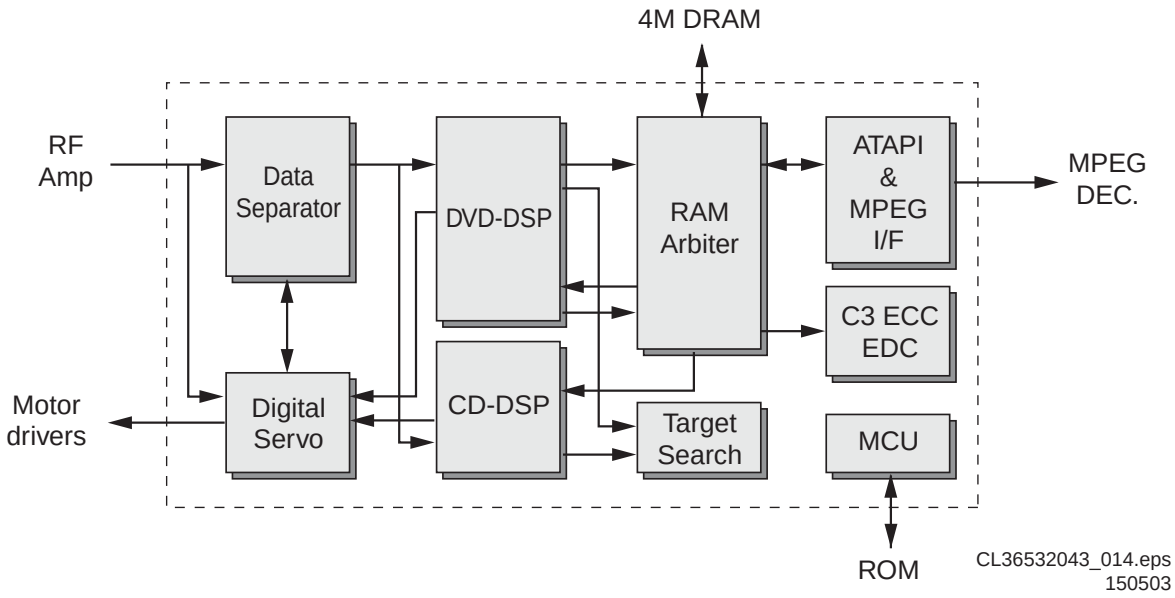


Figure 9-17 Internal Block Diagram and Pin Layout

9.5.5 ZiVA-5 (IC7402)

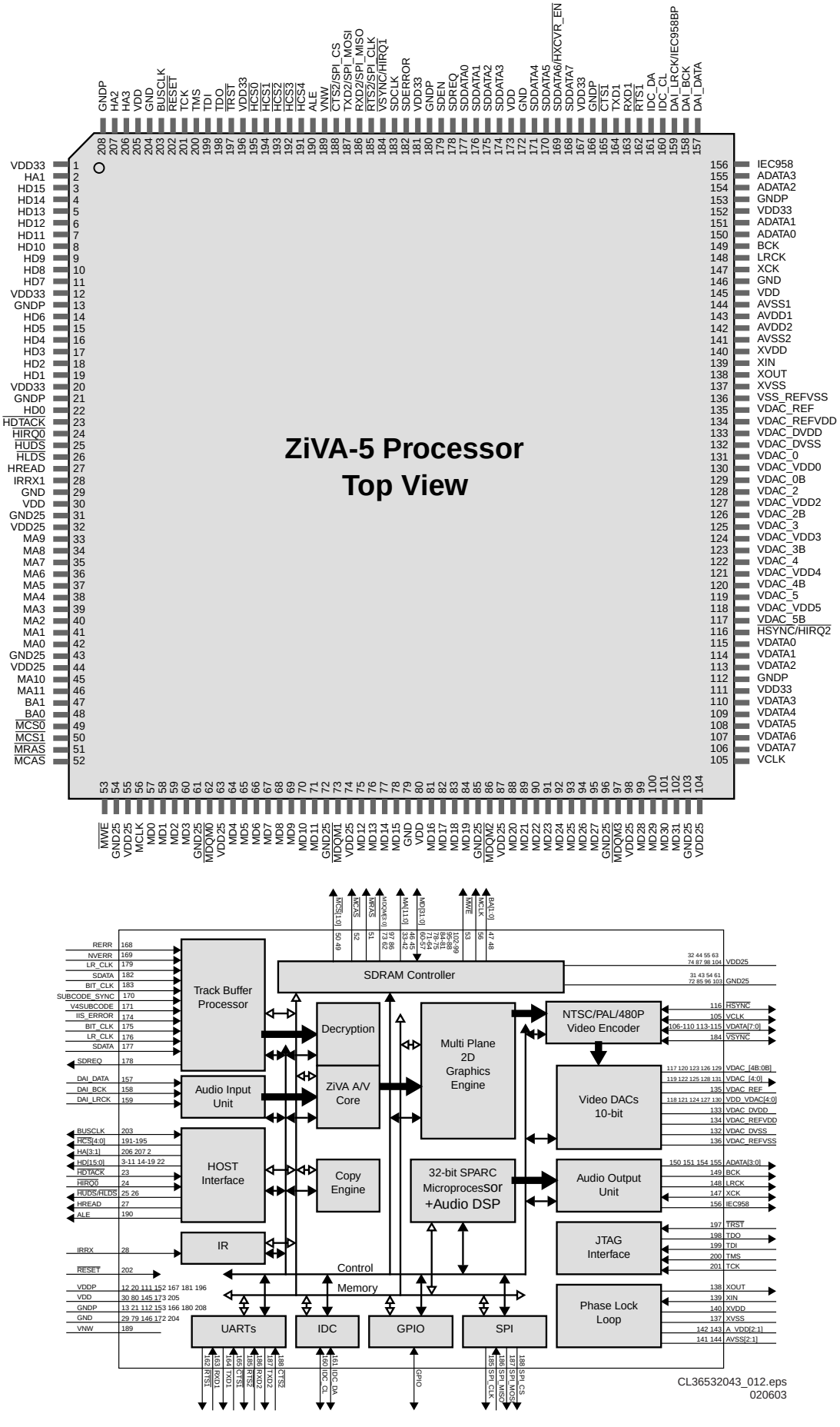


Figure 9-18 Internal Block Diagram and Pin Layout

10. Spare Parts List

DVD M

Various

0001	3139 248 71671	LOADER DVD SLOT-IN TOHEI-PHS

MONO PWB

Various

1001	2422 025 17871	CON BM H 24P F 0.50 FFC 0.3 R
1100	2422 025 17869	CON BM H 15P F 1.00 FFC 0.3 R
1101	2422 025 16542	CON BM H 2P M 2.00 PH SMD R
1102	2422 025 16543	Connector 4P m h 2.00 SMD
1103	2422 025 16835	Connector 3P
1205	2422 543 01338	RES XTL SM 33M8688 20P CX-80 R
1300	2422 025 17599	CON BM H 24P F 1.00 FFC 0.3 R
1301	2422 025 17599	CON BM H 24P F 1.00 FFC 0.3 R
1401	2422 543 01337	RES XTL SM 13M5 12P CX-8045G R
1402	2422 025 16703	CON H 7P M 2.00 PH SMD R
1702	2422 025 16703	CON H 7P M 2.00 PH SMD R
1800	2422 025 17451	CON BM H 30P F 1.00 FFC 0.3 R
1801	2422 086 11103	Fuse SM F 2A 125V
1802	2422 086 11103	Fuse SM F 2A 125V
1803	2422 086 11102	Fuse SM F 1A 125V

⊣⊢

2001	2238 586 59812	100nF 20-80% 50V 0603
2002	5322 124 41945	22µF 20% 35V SMD
2003	2238 586 59812	100nF 20-80% 50V 0603
2004	3198 017 41050	1µF 10V 0603
2005	3198 016 31020	1nF 10% 25V 0603
2006	2238 586 59812	100nF 20-80% 50V 0603
2007	2238 586 59812	100nF 20-80% 50V 0603
2008	3198 016 36810	CER1 0603 NP0 25V 680P COL R
2009	4822 124 12095	100µF 20% 16V
2010	2238 586 59812	100nF 20-80% 50V 0603
2011	2238 586 59812	100nF 20-80% 50V 0603
2012	2238 586 59812	100nF 20-80% 50V 0603
2013	3198 016 36810	CER1 0603 NP0 25V 680P COL R
2014	3198 016 36810	CER1 0603 NP0 25V 680P COL R
2015	3198 016 31020	1nF 10% 25V 0603
2016	3198 016 36810	CER1 0603 NP0 25V 680P COL R
2017	2222 867 15339	33pF 5% 50V 0603
2018	2238 586 59812	100nF 20-80% 50V 0603
2019	2222 867 15339	33pF 5% 50V 0603
2020	3198 016 36810	CER1 0603 NP0 25V 680P COL R
2021	2020 552 94427	100pF 5% 50v 0603
2022	4822 126 13193	4.7nF 10% 63V
2023	2222 867 15339	33pF 5% 50V 0603
2024	3198 017 34730	47nF 16V 0603
2025	4822 124 12095	100µF 20% 16V
2026	2238 586 59812	100nF 20-80% 50V 0603
2027	3198 016 31020	1nF 10% 25V 0603
2028	2238 586 59812	100nF 20-80% 50V 0603
2029	2238 586 59812	100nF 20-80% 50V 0603
2030	2238 586 59812	100nF 20-80% 50V 0603
2032	4822 122 33753	150pF 5% 50V
2033	3198 016 31020	1nF 10% 25V 0603
2034	3198 017 44740	470nF 10V 0603
2035	3198 017 41050	1µF 10V 0603
2036	2222 867 15339	33pF 5% 50V 0603
2037	4822 124 12095	100µF 20% 16V
2038	2238 586 59812	100nF 20-80% 50V 0603
2039	4822 124 12095	100µF 20% 16V
2040	2238 586 59812	100nF 20-80% 50V 0603
2041	4822 124 12095	100µF 20% 16V
2042	3198 016 36810	CER1 0603 NP0 25V 680P COL R
2043	4822 126 13193	4.7nF 10% 63V
2100	2238 586 59812	100nF 20-80% 50V 0603
2101	2238 586 59812	100nF 20-80% 50V 0603
2102	4822 124 23002	10µF 20% 16V
2103	2238 586 59812	100nF 20-80% 50V 0603
2104	2238 586 59812	100nF 20-80% 50V 0603
2105	4822 124 23002	10µF 20% 16V
2106	4822 126 14043	1µF 20% 16V
2107	2020 552 94427	100pF 5% 50v 0603
2108	4822 126 13193	4.7nF 10% 63V
2109	2020 552 94427	100pF 5% 50v 0603
2110	2238 586 59812	100nF 20-80% 50V 0603
2111	2238 586 59812	100nF 20-80% 50V 0603
2112	2238 586 59812	100nF 20-80% 50V 0603
2113	2238 586 59812	100nF 20-80% 50V 0603
2114	2238 586 59812	100nF 20-80% 50V 0603
2115	5322 126 11578	1nF 10% 50V 0603
2116	5322 126 11578	1nF 10% 50V 0603
2117	5322 126 11578	1nF 10% 50V 0603
2118	5322 126 11578	1nF 10% 50V 0603
2119	5322 126 11578	1nF 10% 50V 0603
2120	5322 126 11578	1nF 10% 50V 0603
2121	5322 126 11578	1nF 10% 50V 0603
2200	4822 124 12095	100µF 20% 16V
2201	2238 586 59812	100nF 20-80% 50V 0603
2202	2238 586 59812	100nF 20-80% 50V 0603
2203	2238 586 59812	100nF 20-80% 50V 0603
2204	2238 586 59812	100nF 20-80% 50V 0603
2205	2238 586 59812	100nF 20-80% 50V 0603
2206	2238 586 59812	100nF 20-80% 50V 0603
2207	2238 586 59812	100nF 20-80% 50V 0603
2208	4822 126 11785	47pF 5% 50V 0603
2209	4822 126 14249	560pF 10% 50V 0603
2210	3198 017 34730	47nF 16V 0603
2211	4822 124 12095	100µF 20% 16V
2212	2238 586 59812	100nF 20-80% 50V 0603
2213	2238 586 59812	100nF 20-80% 50V 0603
2214	2238 586 59812	100nF 20-80% 50V 0603
2215	4822 124 12095	100µF 20% 16V
2216	2238 586 59812	100nF 20-80% 50V 0603
2217	2238 586 59812	100nF 20-80% 50V 0603
2218	2238 586 59812	100nF 20-80% 50V 0603
2219	2238 586 59812	100nF 20-80% 50V 0603
2220	2238 586 59812	100nF 20-80% 50V 0603
2221	2238 586 59812	100nF 20-80% 50V 0603
2222	3198 016 31020	1nF 10% 25V 0603
2224	5322 126 11582	6.8nF 10% 63V
2225	3198 017 34730	47nF 16V 0603
2226	3198 017 34730	47nF 16V 0603
2227	4822 126 13881	470pF 5% 50V
2228	4822 126 13881	470pF 5% 50V
2230	2238 586 59812	100nF 20-80% 50V 0603
2231	2238 586 59812	100nF 20-80% 50V 0603
2232	2238 586 59812	100nF 20-80% 50V 0603
2233	3198 016 31020	1nF 10% 25V 0603
2234	3198 016 31020	1nF 10% 25V 0603
2235	3198 016 31020	1nF 10% 25V 0603
2237	4822 124 12084	1µF 20% 50V SMD
2238	4822 124 12084	1µF 20% 50V SMD
2239	4822 122 33761	22pF 5% 50V
2241	4822 122 33761	22pF 5% 50V
2400	2238 586 59812	100nF 20-80% 50V 0603
2401	2238 586 59812	100nF 20-80% 50V 0603
2402	2238 586 59812	100nF 20-80% 50V 0603
2404	4822 124 80151	47µF 20% 16V
2405	2238 586 59812	100nF 20-80% 50V 0603
2406	2238 586 59812	100nF 20-80% 50V 0603
2407	4822 126 11663	12pF 5% 50V 0603
2408	4822 126 11663	12pF 5% 50V 0603
2409	2238 586 59812	100nF 20-80% 50V 0603
2410	4822 122 33761	22pF 5% 50V
2411	4822 122 33761	22pF 5% 50V
2412	4822 122 33761	22pF 5% 50V
2413	4822 122 33761	22pF 5% 50V
2414	4822 122 33761	22pF 5% 50V
2415	4822 122 33761	22pF 5% 50V
2416	4822 122 33761	22pF 5% 50V
2417	4822 122 33761	22pF 5% 50V
2419	2238 586 59812	100nF 20-80% 50V 0603
2420	2238 586 59812	100nF 20-80% 50V 0603
2421	2238 586 59812	100nF 20-80% 50V 0603
2422	2238 586 59812	100nF 20-80% 50V 0603
2423	2238 586 59812	100nF 20-80% 50V 0603
2424	2238 586 59812	100nF 20-80% 50V 0603
2425	2238 586 59812	100nF 20-80% 50V 0603
2426	2238 586 59812	100nF 20-80% 50V 0603
2427	4822 124 80151	47µF 20% 16V
2428	2238 586 59812	100nF 20-80% 50V 0603
2429	2238 586 59812	100nF 20-80% 50V 0603
2430	2238 586 59812	100nF 20-80% 50V 0603
2431	2238 586 59812	100nF 20-80% 50V 0603
2432	2238 586 59812	100nF 20-80% 50V 0603
2433	2238 586 59812	100nF 20-80% 50V 0603
2434	2238 586 59812	100nF 20-80% 50V 0603
2435	2238 586 59812	100nF 20-80% 50V 0603
2436	2238 586 59812	100nF 20-80% 50V 0603
2437	2238 586 59812	100nF 20-80% 50V 0603
2438	2238 586 59812	100nF 20-80% 50V 0603
2439	2238 586 59812	100nF 20-80% 50V 0603
2500	2020 021 91729	4.7µF 20% 35V
2502	2238 586 59812	100nF 20-80% 50V 0603
2503	2238 586 59812	100nF 20-80% 50V 0603
2504	2238 586 59812	100nF 20-80% 50V 0603
2505	4822 124 80151	47µF 20% 16V
2506	2238 586 59812	100nF 20-80% 50V 0603
2507	2238 586 59812	100nF 20-80% 50V 0603
2508	2238 586 59812	100nF 20-80% 50V 0603
2509	2238 586 59812	100nF 20-80% 50V 0603
2510	2238 586 59812	100nF 20-80% 50V 0603
2511	2238 586 59812	100nF 20-80% 50V 0603
2512	2238 586 59812	100nF 20-80% 50V 0603
2513	2238 586 59812	100nF 20-80% 50V 0603
2514	2238 586 59812	100nF 20-80% 50V 0603
2515	2238 586 59812	100nF 20-80% 50V 0603
2516	2238 586 59812	100nF 20-80% 50V 0603
2517	2238 586 59812	100nF 20-80% 50V 0603
2518	2238 586 59812	100nF 20-80% 50V 0603
2519	2238 586 59812	100nF 20-80% 50V 0603
2520	2238 586 59812	100nF 20-80% 50V 0603
2521	4822 122 33741	10pF 10% 50V
2600	2238 586 59812	100nF 20-80% 50V 0603
2601	2238 586 59812	100nF 20-80% 50V 0603
2603	3198 016 36810	CER1 0603 NP0 25V 680P COL R
2609	3198 016 36810	CER1 0603 NP0 25V 680P COL R
2610	4822 124 80151	47µF 20% 16V
2611	2238 586 59812	100nF 20-80% 50V 0603
2613	4822 124 12095	100µF 20% 16V
2614	4822 124 12095	100µF 20% 16V
2615	4822 124 80151	47µF 20% 16V
2617	4822 124 23002	10µF 20% 16V
2618	4822 124 23002	10µF 20% 16V
2619	2238 586 59812	100nF 20-80% 50V 0603
2628	4822 124 80151	47µF 20% 16V
2629	4822 124 80151	47µF 20% 16V
2638	2238 586 59812	100nF 20-80% 50V 0603
2642	5322 124 41945	22µF 20% 35V SMD
2643	2238 586 59812	100nF 20-80% 50V 0603
2649	3198 016 38210	820pF 25V
2650	4822 126 13883	220pF 5% 50V
2651	4822 126 13883	220pF 5% 50V
2652	3198 016 38210	820pF 25V
2653	3198 016 38210	820pF 25V
2656	3198 016 38210	820pF 25V
2669	4822 124 80151	47µF 20% 16V
2670	4822 122 33761	22pF 5% 50V
2671	4822 122 33761	22pF 5% 50V
2672	4822 122 33761	22pF 5% 50V
2674	4822 122 33761	22pF 5% 50V
2675	4822 122 33761	22pF 5% 50V
2676	4822 122 33761	22pF 5% 50V
2677	4822 122 33761	22pF 5% 50V
2679	4822 122 33761	22pF 5% 50V
2680	4822 122 33761	22pF 5% 50V
2708	4822 126 14247	1.5nF 50V 0603
2801	2238 586 59812	100nF 20-80% 50V 0603
2802	4822 122 33741	10pF 10% 50V
2803	4822 122 33741	10pF 10% 50V
2804	2238 586 59812	100nF 20-80% 50V 0603
2805	3198 030 82280	2.2µF 20% 50V
2806	4822 126 14315	390pF 5% 50V 0603
2807	3198 016 38210	820pF 25V
2808	4822 126 14315	390pF 5% 50V 0603
2810	4822 122 33741	10pF 10% 50V
2811	4822 122 33741	10pF 10% 50V
2812	2238 586 59812	100nF 20-80% 50V 0603
2813	3198 030 82280	2.2µF 20% 50V
2814	4822 126 14315	390pF 5% 50V 0603
2815	3198 016 38210	820pF 25V
2816	4822 126 14315	390pF 5% 50V 0603
2817	4822 124 80151	47µF 20% 16V
2818	2238 586 59812	100nF 20-80% 50V 0603
2819	2238 586 59812	100nF 20-80% 50V 0603
2820	4822 124 12095	100µF 20% 16V

2822	4822 122 33741	10pF 10% 50V
2823	4822 122 33741	10pF 10% 50V
2824	2238 586 59812	100nF 20-80% 50V 0603
2826	3198 030 82280	2.2µF 20% 50V
2827	4822 126 14315	390pF 5% 50V 0603
2828	3198 016 38210	820pF 25V
2829	4822 126 14315	390pF 5% 50V 0603
2830	4822 124 12095	100µF 20% 16V
2831	2238 586 59812	100nF 20-80% 50V 0603
2832	4822 124 12095	100µF 20% 16V
2833	2238 586 59812	100nF 20-80% 50V 0603
2835	4822 122 33741	10pF 10% 50V
2836	4822 122 33741	10pF 10% 50V
2837	2238 586 59812	100nF 20-80% 50V 0603
2840	3198 030 82280	2.2µF 20% 50V
2841	4822 124 80151	47µF 20% 16V
2842	2238 586 59812	100nF 20-80% 50V 0603
2843	4822 126 14315	390pF 5% 50V 0603
2844	3198 016 38210	820pF 25V
2845	4822 126 14315	390pF 5% 50V 0603
2846	2238 586 59812	100nF 20-80% 50V 0603
2848	4822 122 33741	10pF 10% 50V
2849	4822 122 33741	10pF 10% 50V
2850	2238 586 59812	100nF 20-80% 50V 0603
2851	2322 704 69109	
2852	3198 030 82280	2.2µF 20% 50V
2853	4822 126 14315	390pF 5% 50V 0603
2854	3198 016 38210	820pF 25V
2855	4822 126 14315	390pF 5% 50V 0603
2856	4822 122 33761	22pF 5% 50V
2857	4822 122 33761	22pF 5% 50V
2858	4822 122 33761	22pF 5% 50V
2859	4822 122 33761	22pF 5% 50V
2860	4822 122 33761	22pF 5% 50V
2861	4822 122 33761	22pF 5% 50V
2862	4822 122 33761	22pF 5% 50V
2863	5322 124 41945	22µF 20% 35V SMD
2864	2238 586 59812	100nF 20-80% 50V 0603
2865	4822 122 33761	22pF 5% 50V
2866	4822 122 33761	22pF 5% 50V

–WW–

3000	4822 051 30109	10Ω 5% 0.062W
3001	2322 704 65102	5.1kΩ 1% 0603
3003	5322 117 13056	8.2K 1% 0.063W 0603
3004	4822 051 30109	10Ω 5% 0.062W
3005	4822 051 30102	1kΩ 5% 0.062W
3006	4822 117 11817	1.2kΩ 1% 1/16W
3007	4822 117 11817	1.2kΩ 1% 1/16W
3008	4822 051 30103	10kΩ 5% 0.062W
3009	4822 051 30103	10kΩ 5% 0.062W
3011	4822 117 11817	1.2kΩ 1% 1/16W
3013	4822 051 30008	Jumper 0603
3014	4822 051 30471	470Ω 5% 0.062W
3016	4822 051 30474	470kΩ 5% 0.062W
3017	4822 051 30103	10kΩ 5% 0.062W
3018	4822 051 30563	56kΩ 5% 0.062W
3019	4822 051 30103	10kΩ 5% 0.062W
3020	4822 051 30472	4.7kΩ 5% 0.062W
3100	4822 051 30689	68Ω 5% 0.063W 0603
3101	4822 051 30333	33kΩ 5% 0.062W
3104	4822 051 20108	1Ω 5% 0.1W
3105	4822 051 30689	68Ω 5% 0.063W 0603
3106	4822 051 30221	220Ω 5% 0.062W
3107	4822 051 20108	1Ω 5% 0.1W
3108	4822 051 30339	33Ω 5% 0.062W
3109	4822 051 30123	12kΩ 5% 0.062W
3110	4822 051 20108	1Ω 5% 0.1W
3111	4822 051 30103	10kΩ 5% 0.062W
3112	4822 051 20108	1Ω 5% 0.1W
3113	4822 051 30332	3.3kΩ 5% 0.062W
3114	4822 051 20108	1Ω 5% 0.1W
3115	4822 051 20108	1Ω 5% 0.1W
3116	4822 117 12925	47kΩ 1% 0.063W 0603
3117	4822 117 12925	47kΩ 1% 0.063W 0603
3118	4822 051 30339	33Ω 5% 0.062W
3120	4822 051 30333	33kΩ 5% 0.062W
3121	4822 051 30221	220Ω 5% 0.062W
3122	4822 051 30333	33kΩ 5% 0.062W
3123	4822 051 30223	22kΩ 5% 0.062W
3124	4822 117 13632	100kΩ 1% 0603 0.62W
3125	4822 051 30221	220Ω 5% 0.062W
3200	2322 704 62003	RST SM 0603 RC22H 20K PM1 R
3203	4822 117 13632	100kΩ 1% 0603 0.62W
3204	2322 704 65102	5.1kΩ 1% 0603
3205	4822 051 30103	10kΩ 5% 0.062W
3207	4822 051 30563	56kΩ 5% 0.062W
3209	4822 117 11817	1.2kΩ 1% 1/16W
3216	4822 051 30472	4.7kΩ 5% 0.062W
3218	4822 117 13576	NETW 4 X 33R 5% 1206
3220	2322 702 60513	RST SM 0603 RC21 51K PM5 R
3224	4822 051 30332	3.3kΩ 5% 0.062W
3225	4822 051 30332	3.3kΩ 5% 0.062W
3226	4822 051 30332	3.3kΩ 5% 0.062W
3227	4822 051 30103	10kΩ 5% 0.062W
3228	4822 051 30339	33Ω 5% 0.062W
3229	4822 117 12925	47kΩ 1% 0.063W 0603
3231	4822 051 30339	33Ω 5% 0.062W
3232	4822 051 30339	33Ω 5% 0.062W
3233	4822 051 30339	33Ω 5% 0.062W
3234	2322 704 65102	5.1kΩ 1% 0603
3235	4822 051 30152	1.5kΩ 5% 0.062W
3236	4822 051 30472	4.7kΩ 5% 0.062W
3238	4822 051 30472	4.7kΩ 5% 0.062W
3239	4822 051 30102	1kΩ 5% 0.062W
3240	4822 051 30223	22kΩ 5% 0.062W
3241	4822 117 12917	1Ω 5% 0.062W 0603
3242	4822 051 30223	22kΩ 5% 0.062W
3244	4822 117 13632	100kΩ 1% 0603 0.62W
3245	4822 051 30222	2.2kΩ 5% 0.062W
3247	4822 051 30103	10kΩ 5% 0.062W
3248	4822 051 30103	10kΩ 5% 0.062W
3400	4822 051 30472	4.7kΩ 5% 0.062W
3401	4822 051 30393	39kΩ 5% 0.062W
3402	4822 051 30393	39kΩ 5% 0.062W
3411	4822 051 30472	4.7kΩ 5% 0.062W
3413	4822 051 30472	4.7kΩ 5% 0.062W
3415	5322 117 13018	1kΩ 1% 0.063W 0603
3417	4822 051 30339	33Ω 5% 0.062W
3419	4822 051 30339	33Ω 5% 0.062W
3420	4822 051 30472	4.7kΩ 5% 0.062W
3421	4822 051 30339	33Ω 5% 0.062W
3422	4822 051 30339	33Ω 5% 0.062W
3424	4822 051 30339	33Ω 5% 0.062W
3425	4822 051 30339	33Ω 5% 0.062W
3427	4822 051 30339	33Ω 5% 0.062W
3428	4822 051 30339	33Ω 5% 0.062W
3431	4822 051 30472	4.7kΩ 5% 0.062W
3432	4822 051 30689	68Ω 5% 0.063W 0603
3433	4822 051 30689	68Ω 5% 0.063W 0603
3436	4822 051 30472	4.7kΩ 5% 0.062W
3439	4822 051 30339	33Ω 5% 0.062W
3440	4822 051 30339	33Ω 5% 0.062W
3443	4822 051 30339	33Ω 5% 0.062W
3445	4822 051 30339	33Ω 5% 0.062W
3448	4822 051 30339	33Ω 5% 0.062W
3451	4822 051 30472	4.7kΩ 5% 0.062W
3464	4822 117 13576	NETW 4 X 33R 5% 1206
3465	4822 117 13576	NETW 4 X 33R 5% 1206
3466	4822 117 13576	NETW 4 X 33R 5% 1206
3467	4822 117 13576	NETW 4 X 33R 5% 1206
3468	4822 117 13576	NETW 4 X 33R 5% 1206
3470	4822 117 13576	NETW 4 X 33R 5% 1206
3471	4822 117 13576	NETW 4 X 33R 5% 1206
3472	4822 117 13576	NETW 4 X 33R 5% 1206
3473	4822 051 30339	33Ω 5% 0.062W
3474	4822 117 13576	NETW 4 X 33R 5% 1206
3475	4822 051 30339	33Ω 5% 0.062W
3476	4822 051 30339	33Ω 5% 0.062W
3477	4822 051 30339	33Ω 5% 0.062W
3478	5322 117 13061	180Ω 1% 0.063W 0603
3479	4822 051 30103	10kΩ 5% 0.062W
3480	4822 051 30105	1MΩ 5% 0.062W
3500	4822 051 30472	4.7kΩ 5% 0.062W
3503	4822 117 12917	1Ω 5% 0.062W 0603
3504	4822 051 30472	4.7kΩ 5% 0.062W
3505	4822 051 30472	4.7kΩ 5% 0.062W
3506	4822 117 12917	1Ω 5% 0.062W 0603
3507	4822 051 30101	100Ω 5% 0.062W
3508	4822 117 12917	1Ω 5% 0.062W 0603
3620	4822 051 30222	2.2kΩ 5% 0.062W
3621	5322 117 13037	2.2kΩ 0.063W 0603
3622	5322 117 13018	1kΩ 1% 0.063W 0603
3623	4822 051 30101	100Ω 5% 0.062W
3624	5322 117 13037	2.2kΩ 0.063W 0603
3625	5322 117 13018	1kΩ 1% 0.063W 0603
3626	4822 051 30222	2.2kΩ 5% 0.062W
3627	4822 051 30103	10kΩ 5% 0.062W
3628	5322 117 13051	680R 1% 0.063W 0603
3629	4822 051 30222	2.2kΩ 5% 0.062W
3630	4822 051 30103	10kΩ 5% 0.062W
3631	4822 051 30222	2.2kΩ 5% 0.062W
3632	5322 117 13037	2.2kΩ 0.063W 0603
3633	5322 117 13018	1kΩ 1% 0.063W 0603
3635	4822 051 30103	10kΩ 5% 0.062W
3636	4822 051 30103	10kΩ 5% 0.062W
3637	4822 051 30101	100Ω 5% 0.062W
3638	4822 051 30103	10kΩ 5% 0.062W
3639	5322 117 13037	2.2kΩ 0.063W 0603
3640	5322 117 13018	1kΩ 1% 0.063W 0603
3641	4822 051 30222	2.2kΩ 5% 0.062W
3642	4822 051 30223	22kΩ 5% 0.062W
3643	4822 051 30222	2.2kΩ 5% 0.062W
3644	5322 117 13051	680R 1% 0.063W 0603
3645	4822 051 30103	10kΩ 5% 0.062W
3665	4822 051 30103	10kΩ 5% 0.062W
3671	4822 051 30103	10kΩ 5% 0.062W
3672	4822 051 30223	22kΩ 5% 0.062W
3673	4822 051 30103	10kΩ 5% 0.062W
3674	4822 051 30103	10kΩ 5% 0.062W
3675	4822 051 30689	68Ω 5% 0.063W 0603
3676	4822 051 30222	2.2kΩ 5% 0.062W
3677	4822 051 30103	10kΩ 5% 0.062W
3678	4822 051 30222	2.2kΩ 5% 0.062W
3679	4822 051 30222	2.2kΩ 5% 0.062W
3700	4822 051 30472	4.7kΩ 5% 0.062W
3710	4822 051 30102	1kΩ 5% 0.062W
3711	4822 051 30101	100Ω 5% 0.062W
3712	4822 051 30472	4.7kΩ 5% 0.062W
3713	4822 051 30103	10kΩ 5% 0.062W
3714	4822 051 30103	10kΩ 5% 0.062W
3716	4822 051 30682	6.8kΩ 5% 0.062W
3717	4822 051 30103	10kΩ 5% 0.062W
3727	2120 108 94059	RST NETW SM RAC16 4X JUMPER R
3728	2120 108 94059	RST NETW SM RAC16 4X JUMPER R
3729	2120 108 94059	RST NETW SM RAC16 4X JUMPER R
3730	2120 108 94059	RST NETW SM RAC16 4X JUMPER R
3731	2120 108 94059	RST NETW SM RAC16 4X JUMPER R
3732	2120 108 94059	RST NETW SM RAC16 4X JUMPER R
3733	4822 051 30472	4.7kΩ 5% 0.062W
3734	4822 051 30472	4.7kΩ 5% 0.062W
3735	4822 051 30103	10kΩ 5% 0.062W
3801	4822 051 30563	56kΩ 5% 0.062W
3802	4822 051 30471	470Ω 5% 0.062W
3803	4822 051 30101	100Ω 5% 0.062W
3804	4822 051 30221	220Ω 5% 0.062W
3805	4822 051 30689	68Ω 5% 0.063W 0603
3806	5322 117 13055	75R 1% 0.063W 0603
3807	4822 051 30153	15kΩ 5% 0.062W
3808	4822 051 30221	220Ω 5% 0.062W
3809	4822 051 30563	56kΩ 5% 0.062W
3810	4822 051 30471	470Ω 5% 0.062W
3811	4822 051 30101	100Ω 5% 0.062W
3813	4822 051 30221	220Ω 5% 0.062W
3814	4822 051 30689	68Ω 5% 0.063W 0603
3815	5322 117 13055	75R 1% 0.063W 0603
3816	4822 051 30153	15kΩ 5% 0.062W
3817	4822 051 30221	220Ω 5% 0.062W
3820	4822 051 30563	56kΩ 5% 0.062W
3821	4822 051 30471	470Ω 5% 0.062W
3822	4822 051 30101	100Ω 5% 0.062W
3824	4822 051 30221	220Ω 5% 0.062W
3825	4822 051 30689	68Ω 5% 0.063W 0603
3826	5322 117 13055	75R 1% 0.063W 0603
3827	4822 051 30153	15kΩ 5% 0.062W
3828	4822 051 30221	220Ω 5% 0.062W
3829	4822 051 30563	56kΩ 5% 0.062W
3830	4822 051 30471	470Ω 5% 0.062W
3831	4822 051 30101	100Ω 5% 0.062W
3833	4822 051 30221	220Ω 5% 0.062W
3834	4822 051 30689	68Ω 5% 0.063W 0603
3835	5322 117 13055	75R 1% 0.063W 0603
3836	4822 051 30153	15kΩ 5% 0.062W
3837	4822 051 30221	220Ω 5% 0.062W
3838	4822 051 30331	330Ω 5% 0.062W
3839	4822 051 30563	56kΩ 5% 0.062W
3840	4822 051 30471	470Ω 5% 0.062W
3841	4822 051 30101	100Ω 5% 0.062W
3843	4822 051 30221	220Ω 5% 0.062W
3844	4822 051 30689	68Ω 5% 0.063W 0603
3845	5322 117 13055	75R 1% 0.063W 0603
3846	4822 051 30153	15kΩ 5% 0.062W
3847	4822 051 30221	220Ω 5% 0.062W
3848	5322 117 13055	75R 1% 0.063W 0603
3849	5322 117 13055	75R 1% 0.063W 0603
3850	5322 117 13055	75R 1% 0.063W 0603
3851	5322 117 13055	75R 1% 0.063W 0603
3852	5322 117 13055	75R 1% 0.063W 0603
3855	4822 117 11748	2.2Ω 1206 5%
3856	4822 117 11748	2.2Ω 1206 5%
3861	4822 117 11748	2.2Ω 1206 5%
4000	4822 051 30008	Jumper 0603
4102	4822 051 30008	Jumper 0603
4105	4822 051 30008	Jumper 0603
4107	4822 051 30008	Jumper 0603
4108	4822 051 30008	Jumper 0603
4203	4822 051 30008	Jumper 0603
4405	4822 051 30008	Jumper 0603
4605	2322 704 62001	RST SM 0603 RC22H 200R PM1 R

4606	2322 704 62001	RST SM 0603 RC22H 200R PM1 R
4616	4822 051 30008	Jumper 0603
4619	4822 051 30008	Jumper 0603
4712	4822 051 30008	Jumper 0603
4713	4822 051 30008	Jumper 0603
4807	4822 051 30008	Jumper 0603
4811	4822 051 30008	Jumper 0603
4813	4822 051 30008	Jumper 0603
4814	4822 051 30008	Jumper 0603
4817	4822 051 30008	Jumper 0603
4818	4822 051 30008	Jumper 0603
4819	4822 051 30008	Jumper 0603

5000	2422 536 00215	10µH 5%
5001	2422 536 00215	10µH 5%
5002	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5100	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5101	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5102	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5103	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5104	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5105	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5106	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5107	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5200	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5201	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5202	2422 549 45186	IND FXD 0805 EMI 100MHZ 60R R
5203	2422 549 45186	IND FXD 0805 EMI 100MHZ 60R R
5204	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5400	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5401	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5402	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5403	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5408	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5409	2422 549 45186	IND FXD 0805 EMI 100MHZ 60R R
5500	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5501	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5603	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5605	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5607	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5611	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5612	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5613	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5614	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5615	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5616	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5704	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5800	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5801	4822 157 10586	2.2µH 10% 0805
5802	4822 157 10586	2.2µH 10% 0805
5803	4822 157 10586	2.2µH 10% 0805
5804	4822 157 10586	2.2µH 10% 0805
5805	4822 157 10586	2.2µH 10% 0805
5806	4822 157 10586	2.2µH 10% 0805
5807	4822 157 10586	2.2µH 10% 0805
5808	4822 157 10586	2.2µH 10% 0805
5809	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5810	4822 157 10586	2.2µH 10% 0805
5811	4822 157 10586	2.2µH 10% 0805
5813	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5815	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5817	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5818	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5821	2422 549 45618	IND FXD 0603 EMI 100MHZ 60R R
5823	2422 549 45619	IND FXD 1206 EMI 100MHZ 60R R

6000	4822 130 11397	BAS316
6001	4822 130 11397	BAS316
6100	4822 130 11397	BAS316
6201	4822 130 11397	BAS316
6202	4822 130 11397	BAS316
6400	4822 130 11397	BAS316
6603	4822 130 11397	BAS316
6604	4822 130 11397	BAS316
6605	4822 130 11397	BAS316
6606	4822 130 11397	BAS316
6803	9322 128 69685	S1D
6804	9322 128 69685	S1D
6805	9322 128 69685	S1D
6806	9322 128 69685	S1D
6807	9322 128 69685	S1D
6808	9322 128 69685	S1D
6810	4822 130 11416	PDZ6.8B
6811	4822 130 11416	PDZ6.8B
6812	4822 130 11416	PDZ6.8B
6813	4822 130 11416	PDZ6.8B

7000	4822 130 11565	2SB1132
7001	4822 130 11565	2SB1132
7002	9322 185 60671	IC SM SP3721AAA0PM (TI00) Y
7003	4822 209 32073	MC34072D
7100	9322 187 63668	IC SM BA5954FP(RHM0) R
7101	9322 187 64668	IC SM BA6849FP (RHM0) R
7200	9322 186 11671	IC SM M5705 (ACLI) Y
7201	9322 174 02668	AS4C256K16E0-60JC
7202	9965 000 18147	M29F002BT/100301
7203	5322 130 60159	BC846B
7400	9322 130 41668	IC SM M24C64-WMN6 (ST00) R
7401	9352 190 10118	IC SM 74LVC573ADB (PHSE) R
7402	9322 195 06671	IC SM ZIVA-5M (LLC0) Y
7403	9352 190 10118	IC SM 74LVC573ADB (PHSE) R
7404	9352 190 10118	IC SM 74LVC573ADB (PHSE) R
7406	9965 000 04199	BSN20
7407	9965 000 04199	BSN20
7500	9322 163 29685	IC SM NCP303LSN45 (ONSE) R
7501	9965 000 18136	M29W160DT-70N1/VER SD5.31-18
7502	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRN0)R
7503	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRN0)R
7600	9322 148 78668	IC SM AD1852JRS (ANA0) R
7601	4822 130 42804	BC817-25
7602	4822 209 30095	LM833D
7603	4822 130 42804	BC817-25
7605	4822 130 60373	BC856B
7606	5322 130 60159	BC846B
7607	4822 130 60373	BC856B
7608	4822 130 60373	BC856B
7609	4822 130 60373	BC856B
7614	4822 209 30095	LM833D
7615	4822 130 60373	BC856B
7702	9340 425 20115	BC847BS
7800	9340 425 30115	BC847BPN
7803	9340 425 30115	BC847BPN
7804	9322 167 69668	IC SM LD1117ADT18 (ST00) R
7806	9340 425 30115	BC847BPN
7807	9322 194 23668	IC SM LF90CDT (ST00) R
7809	9340 425 30115	BC847BPN
7810	9352 456 80115	74HCT1G125GW
7812	9340 425 30115	BC847BPN
7814	4822 209 90927	L78L05ACD

11. Revision List

First release